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66	Power-6:+VCCGT Driver
67	Power-7:+VCCSA
68	Power-8:+VCCIO
69	Power-9+1P0V_PCH_AUX
70	Power-10:+3P3V_SB/+5V_AUX
71	Power-11:-12V
72	Power-12:DDR3 +1P35V_VDDQ
73	
74	
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77	
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Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

DO NOT DISTRIBUTE

BOM	Version
LNI	WW TPM(NUVOTON)
NLI	EM TPM(NATIONZ)

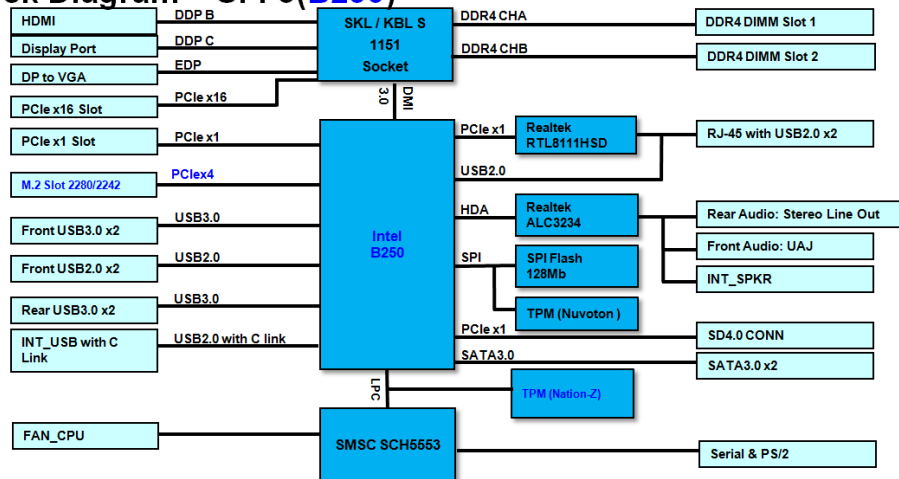
Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List


PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

	
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DRWG NO D8 SFF 3	Rev A00
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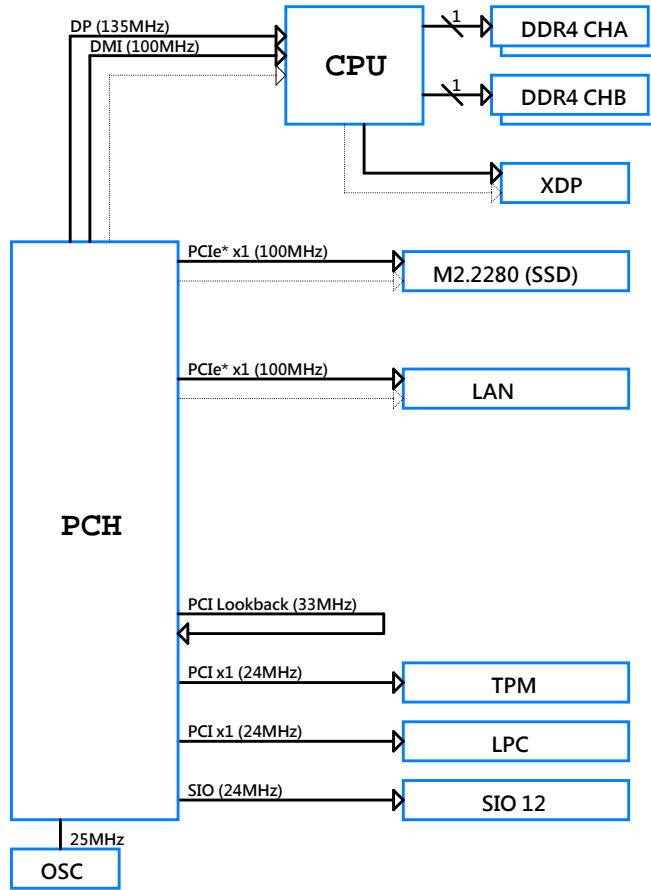
MB Block Diagram – SFF3(B250)



		
Title		
Block Diagram		
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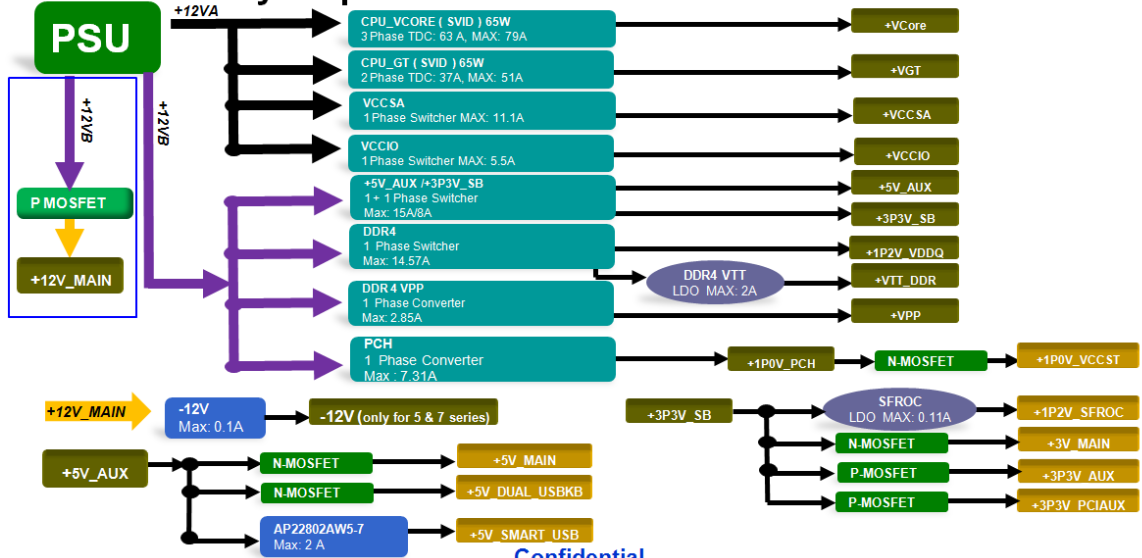
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Clock Diagram



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CLOCKS		
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Power Delivery Map



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HP Restricted Document

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Figure 41-3. KBL-S Timing Diagram for G3 to S0/M0 [Deep Sx Platform] (Sheet 1 of 2)

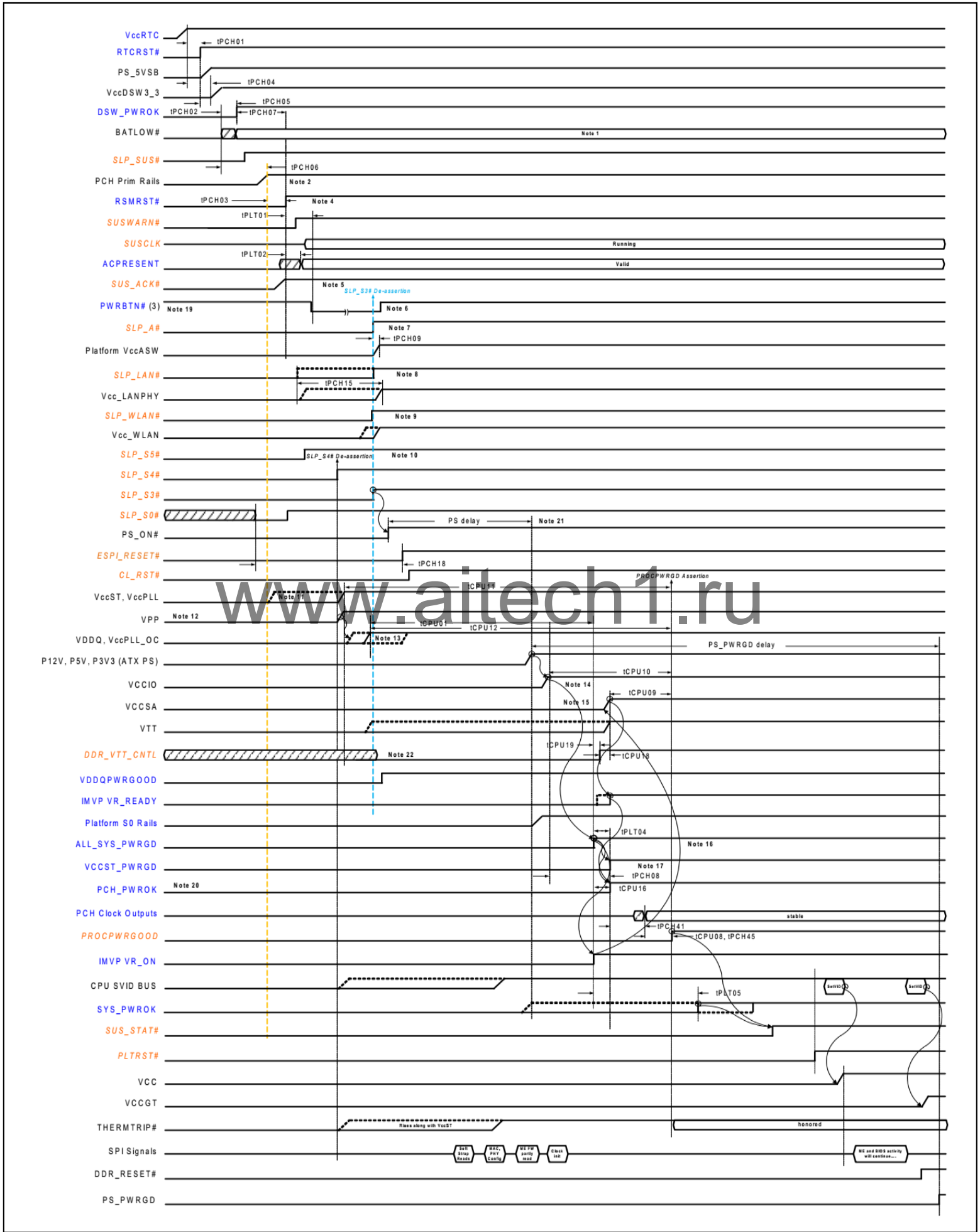
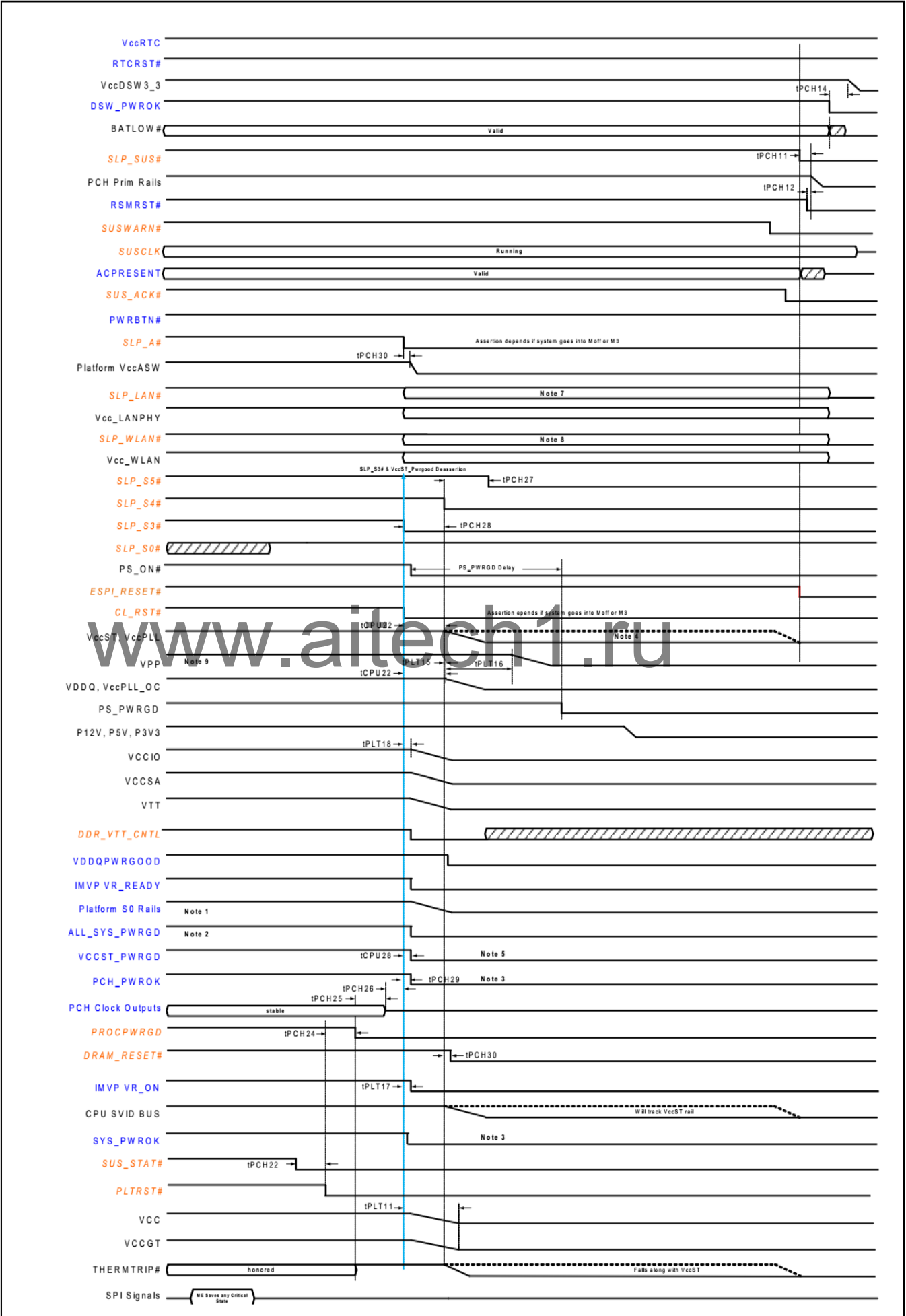

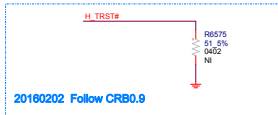


Figure 41-5. KBL-S Timing Diagram for S0/M0 to G3 [Deep Sx Platform]

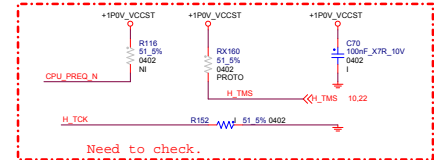


	
Title Interrupt & PME	
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20140520 Need check Debug port PDG



Intel MCP XDP Debug Connector

PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.
place R148,R149 close to CPU
20140520 Follow CRB0.5 and PDG0.7

C68 is dummy R148, R149
PDG is Pop R148, R149

20140520 Follow CRB0.5 and PDG0.7

Need to connect to PCH JTAG pin

20140519 Follow CRB0.5 and PDG0.7

Note 1:
VCCST Power Gating (Q1) implemented: XDP_PRESENT# need connect to Q1.G with a inverse logic.

DCI input L XDP DEFAULT

1. For TDI
Delete the RX161
2. For TDO
Delete the RX162
Change the RX175 from 100 ohm to 51 ohm
3. For TMS
Delete the RX160
4. For PRDY# and PREQ#
Stuff the R148/R149



CPU-XDP		
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FOXCONN CONFIDENTIAL

20140508 The resistors value of SVID follow CRB0.5 and PDG0.7

Need to check VR control power level, Level Shift?

+1P0V_VCCST C R51 10K 5% 0402 H_CATERM#
+1P0V_VCCST C R52 10K 5% 0402 VR_HOT

20140516 CRB0.5 add RS 33 ohm, but PDG0.7 is 20 ohm, need check Intel
20140519 Need check with Intel about RS value. CRB is 0 ohm, PDG0.7 is 500 ohm
20140519 Change net name to H_SKTOCC#

+VCCIO_056 10K 5% 0402 CPU_SELECT#
20140520 PU EDS0.75 "Stiff R47 for Enable eDP, unstuff R38, R1 for PCIe X16
20140520 EDS0.75 CFG(18:8): Reserved configuration lanes.

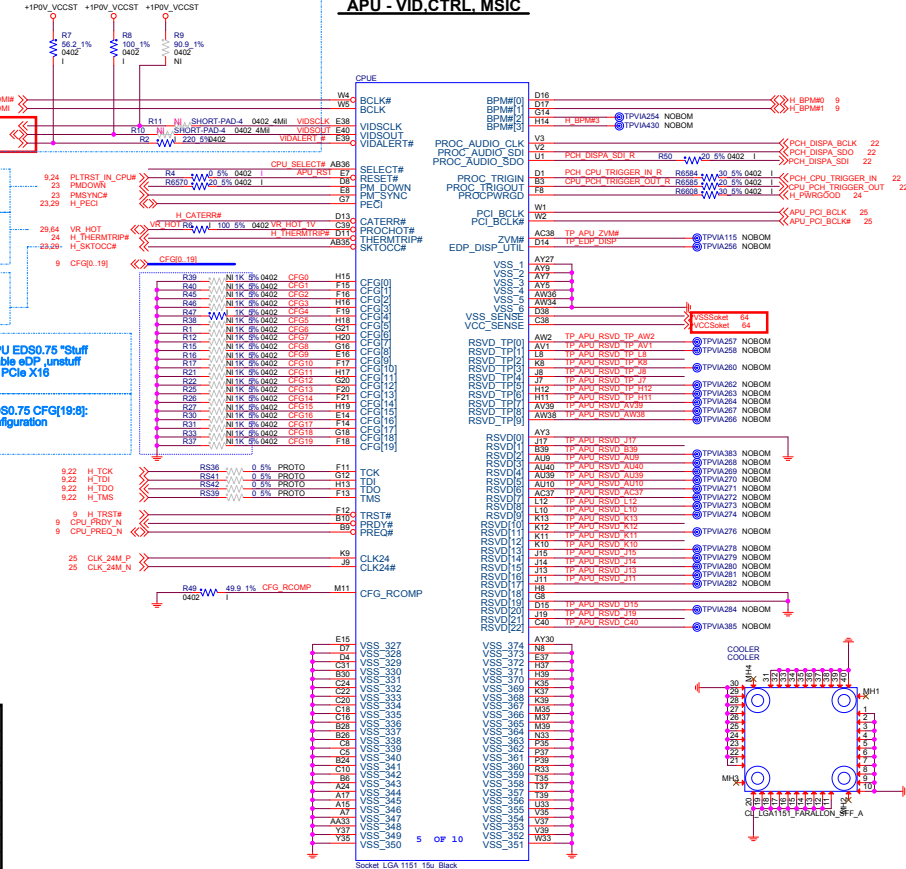
SEL S has adequate internal bias resistance on JTAG. PROC_PROVIDE to keep the devices in an idle state without the external pull resistors.

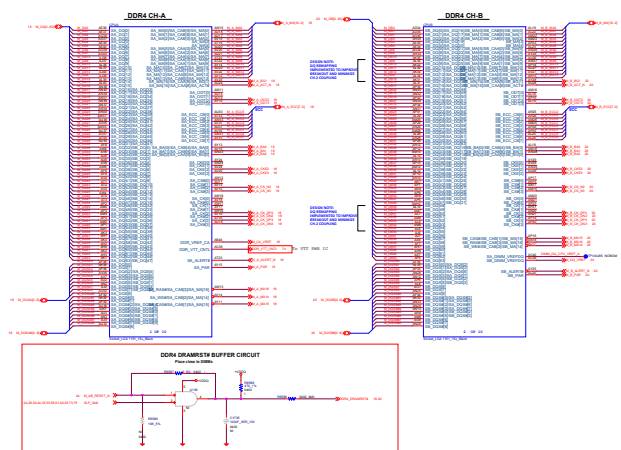
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	BAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG LANE REVERSAL
3	DISABLE	DISABLE	PHYSICAL DEBUG ENABLE
4	DISABLE	ENABLE	eDP en/dis
5	DISABLE	ENABLE	PRDCCPOSEL[0]
6	DISABLE	ENABLE	PRDCCPOSEL[1]
7	RESET_N	BIOS_PRO	PRD DEFER TRAINING
8	DISABLE	ENABLE	CFG INLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFIR MODE ROOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

APU - VID_CTRL_MSIC






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D8-SFF3_B00_SCH_1130_20151029
Base on D7-SFF3_X02_A_SCH_1600_20150917
1.Combine DC cost down schematic(2015_1018A).

D8-SFF3_B00_SCH_1630_20151029
Base on D8-SFF3_B00_SCH_1130_20151029
1.EE Cost Down base on D8 cost down list.

D8-SFF3_B00_SCH_1930_20151030
Base on D8-SFF57_B00_SCH_1630_20151029
1.Update SYS&CPU FAN CONN on page46.

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MCP - PCIE,DMI,FDI,DDI

Part No.	Cap	Value
Cap1	100pF	100pF
Cap2	100pF	100pF

PEG x16 & DMI - Refer to PDG page45

Breakout

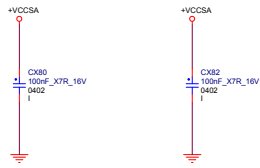
MS = 10/4/4/4/10

DEL = 10/3/3.5/3/10

Main

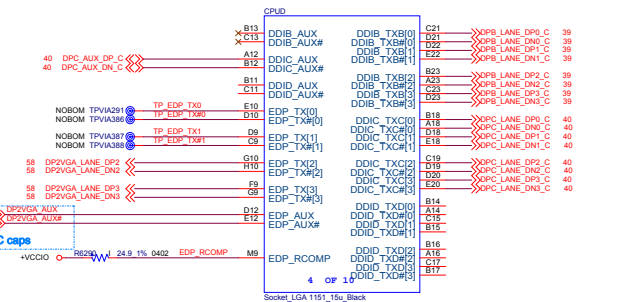
12/3/5/4/5/3.5/12 (Group)

15/3/5/4/5/3.5/15 (Other)



PEG_RCOMP:
Trace Width = 12 mils
Spacing = 15 mils
Length = 400mils

+VCCIO R239 24.9 1% 0402 PEGIOCOMP MCP L7
PEG_RCOMP 3 OF 10
Socket_LGA1151_1su_Black



20140515 remove duplicated AC caps

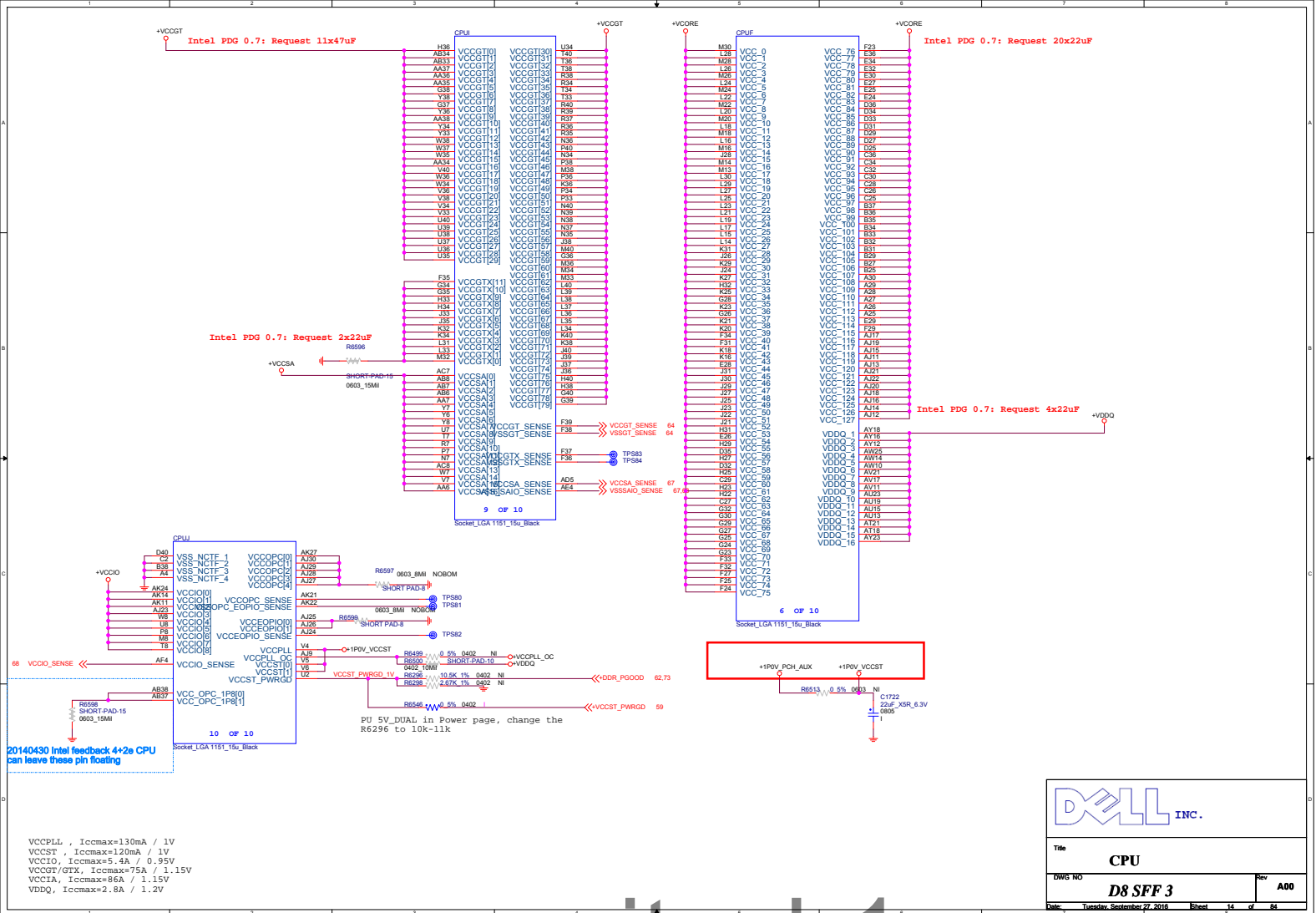
+VCCIO R239 24.9 1% 0402 EDP_RCOMP M5
EDP_RCOMP 4 OF 10
Socket_LGA1151_1su_Black

Parameter	Units	Trace width	Trace spacing	Routing length	Resistance
PEG_RCOMP	mils	12	15	400	
Resistor	ohm				24.9±1%

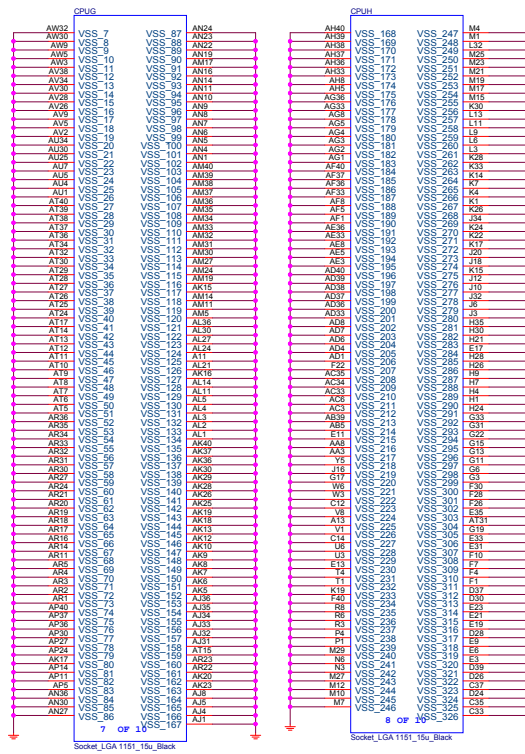


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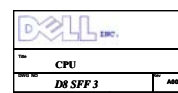
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
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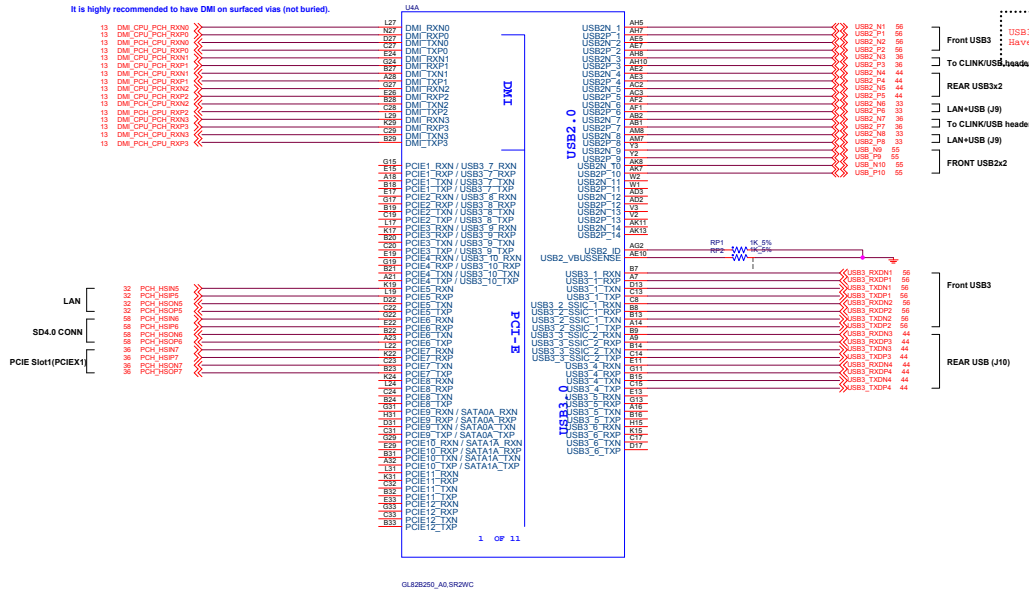


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It is highly recommended to have DMI on surfaced vias (not buried).



ARD1.06 PCH I/O Port Mapping

Port#	Intel	3 Series PCH, H110	7/9 Series PCH, Q170
1	USB1#1	USB3 Front USB3 conn.	USB3 Front USB3 conn.
2	USB1#2	USB3 Front USB3 conn.	USB3 Front USB3 conn.
3	USB1#3	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
4	USB1#4	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
5	USB1#5	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
6	USB1#6	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
7	USB1#7/PCIEX1	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
8	USB1#8/PCIEX2	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
9	USB1#9/PCIEX3	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
10	USB1#10/PCIEX4/GbE	USB3 Rear USB3 conn.	USB3 Rear USB3 conn.
11	PCIEX5/GbE	PCIe NIC	PCIe Intel NIC
12	PCIEX6	SD 4.0 CR	PCIe SD 4.0 CR
13	PCIEX7	PCIe slot 1 (x4)	PCIe slot 1 (x4)
14	PCIEX8	PCIe M.2 WLAN*	PCIe M.2 WLAN*
15	PCIEX9/SATA0/GbE	PCIe	PCIe M.2 SATA0/GbE
16	PCIEX10/SATA1	PCIe	PCIe slot 1 (x4)
17	PCIEX11	PCIe	PCIe slot 1 (x4)
18	PCIEX12/GbE	PCIe	PCIe slot 1 (x4)
19	PCIEX13/SATA0/GbE	SATA HDD1	SATA HDD1
20	PCIEX14/SATA1	SATA HDD2/ODD	SATA HDD2/ODD
21	PCIEX15/SATA2	SATA	SATA HDD3
22	PCIEX16/SATA3	SATA M.2 SSD*	SATA M.2 SSD*
23	PCIEX17/SATA4	SATA/PCIe	SATA/PCIe M.2 SSD SATA/PCIe lane 1
24	PCIEX18/SATA5	SATA/PCIe	SATA/PCIe M.2 SSD SATA/PCIe lane 2
25	PCIEX19	PCIe	PCIe M.2 SSD SATA/PCIe lane 3
26	PCIEX20	PCIe	PCIe M.2 SSD SATA/PCIe lane 4

USB Pin Assignment						
USB Port	Pin Name	Pin Type	USB OC Port	Y/N	Note	Location
1	USB2N1-P1	IN OUT	USB_OC_R_N	Y	Front USB3.0	USB1F2 port1
2	USB2N2-P2	IN OUT	USB_OC_R_N	Y	Front USB3.0	USB1F2 port2
3	USB2N4-P4	IN OUT	USB_OC_L_R_N	Y	Rear USB 3.0/4 Down	USB1R1 port 1
4	USB2N5-P5	IN OUT	USB_OC_L_R_N	Y	Rear USB 3.0/4 Down	USB1R1 port 2
5	USB2N7-P7	IN OUT	USB_OC_L_R_N	Y	Rear USB 3.0/4 up	USB1R1 port 3
6	USB2N8-P8	IN OUT	USB_OC_L_R_N	Y	Rear USB 3.0/4 up	USB1R1 port 4
7	USB2N9-P9	IN OUT	USB_OC_L_R_N	Y	R245-Rear USB2.0 W/ Smart port on R244 USB port1	USB1R1 port1
8	USB2N10-P10	IN OUT	USB_OC_L_R_N	Y	R245-Rear USB2.0 W/ Smart port on R244 USB port2	USB1R1 port2
9	USB2N11-P11	IN OUT	USB_OC_L_R_N	Y	Front USB2.0 W/O CHARGER	USB1F1 port1
10	USB2N12-P12	IN OUT	USB_OC_L_R_N	Y	Front USB2.0 W/O CHARGER	USB1F1 port2
11	USB2N13-P13	IN OUT	N/A	N/A	N/A	N/A
12	USB2N14-P14	IN OUT	USB_OC_L_R_N	Y	CLINK/USB HEADER	CLINK1 port1
13	USB2N15-P15	IN OUT	USB_OC_L_R_N	Y	CLINK/USB HEADER	CLINK1 port2
14	USB2N16-P16	IN OUT	USB_OC_L_R_N	Y	N/A	N/A

FAN USB Port Mapping				
USB3 Port#	USB2.0	USB3.0	Function	Note
Port1	USB2P1	USB3T1 USB3T1a1	Front USB3.0	
Port2	USB2P2	USB3T2 USB3T2a2	Front USB3.0	
Port3	USB2P3	USB3T3 USB3T3a3	Rear USB3.0/4 down	
Port4	USB2P4	USB3T4 USB3T4a4	Rear USB3.0/4 down	
Port5	USB2P5	USB3T5 USB3T5a5	Rear USB3.0/4 up	SFF3: CLINK/HT
Port6	USB2P6	USB3T6 USB3T6a6	Rear USB3.0/4 up	

TITLE

PCH

DWG NO

D8 SFF 3

Rev

A00

Date

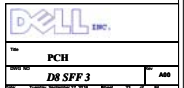
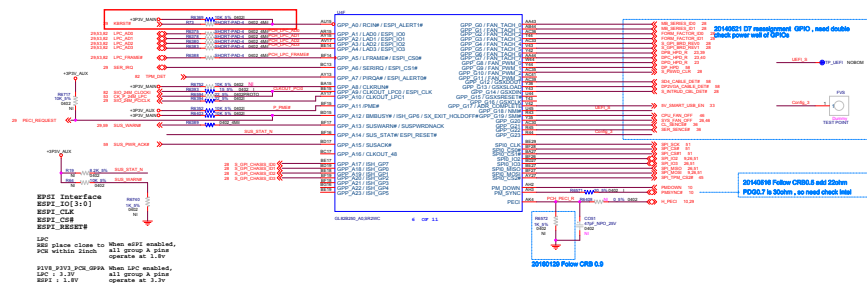
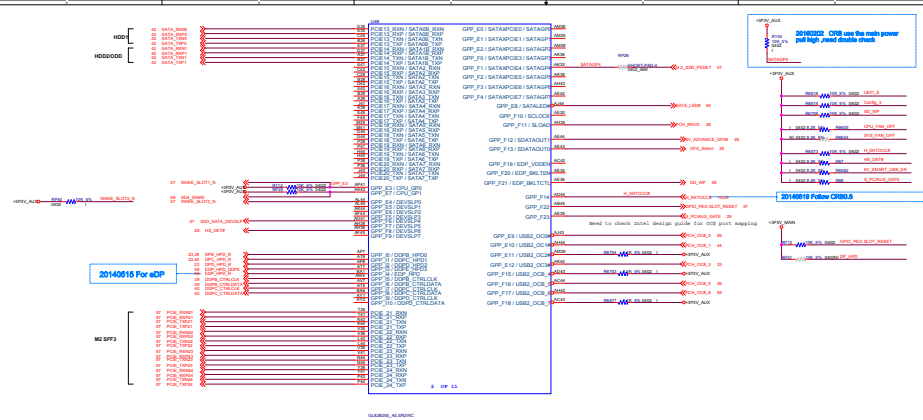
Tuesday, September 27, 2016

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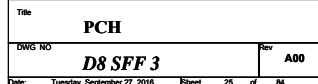
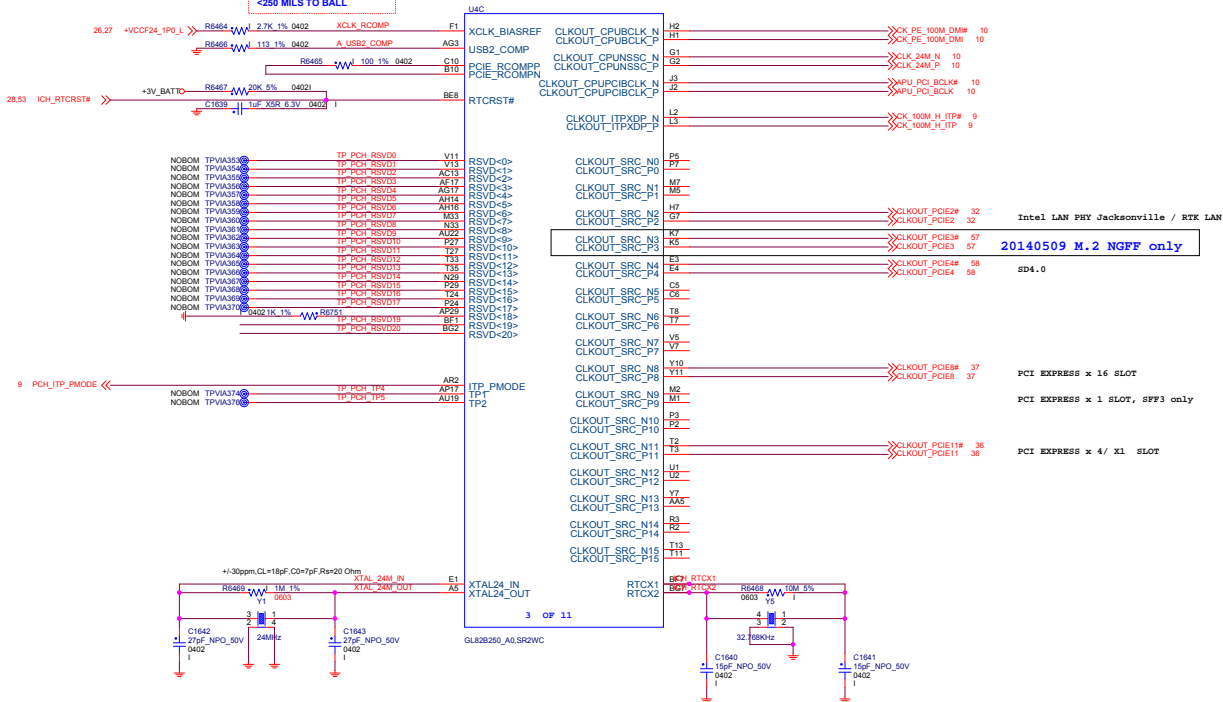
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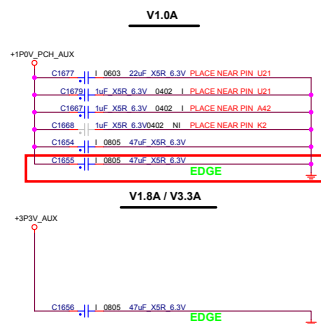
of

21



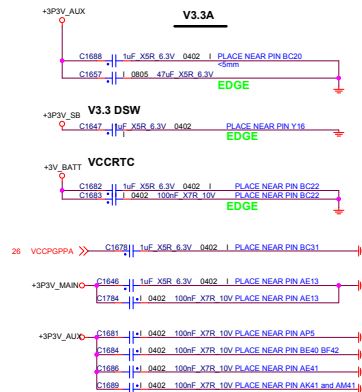
**PLACE CLOSE TO PCH
<250 MILS TO BALL**



FILTER

Need to update for SLK

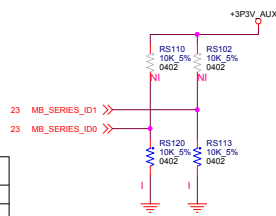
Voltage	Interface	PCB Pins sharing power rail
VCC_PCB 1.05V	Core	V26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	P19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	SPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 M14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AF22
	SUB	AM33, AM33
PCB 3.3V Standby	USB2	AM18, AM20, AM22, AJ20, AK20
	ASALIA	AM26
	USB3	P20
	RTC	AP35
PCB 3.3V	CLK	AM7, AM9, AP5, AP7, AK4, AT5, AV4, AM4, AM9, AG12, AK11,
	RVCN08	AG1
	PCIe	AV3, AM3
	Core	U30, W30
	Fuse	AF26



Title		PCH	
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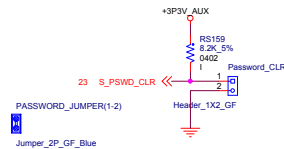
MB series ID

ID1	ID0	Type
0	0	SFF3
0	1	SFF5
1	0	SFF7
1	1	Farallon



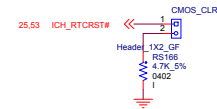
Clear Password

Password_CLR	SHORT : DEFAULT
	OPEN : Password RESET



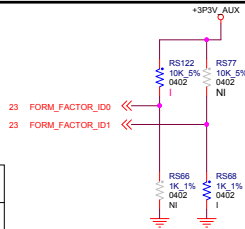
CLR_CMOS

CMOS_CLR	SHORT : CMOS RESET
	OPEN : DEFAULT

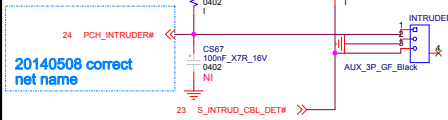


Form Factor ID

ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro

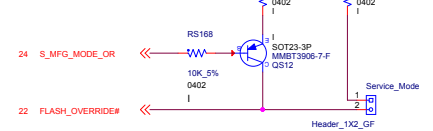


Chassis Intruder



ME Disable (Flash override)

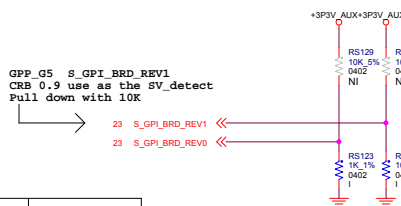
QS12 circuit for BIOS control



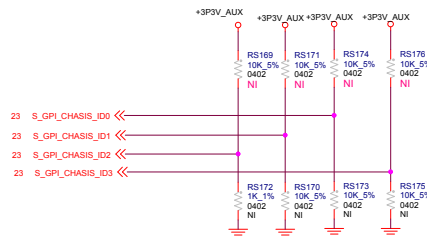
Service_Mode	SHORT : ME DISABLE
	OPEN : DEFAULT

BOARD ID

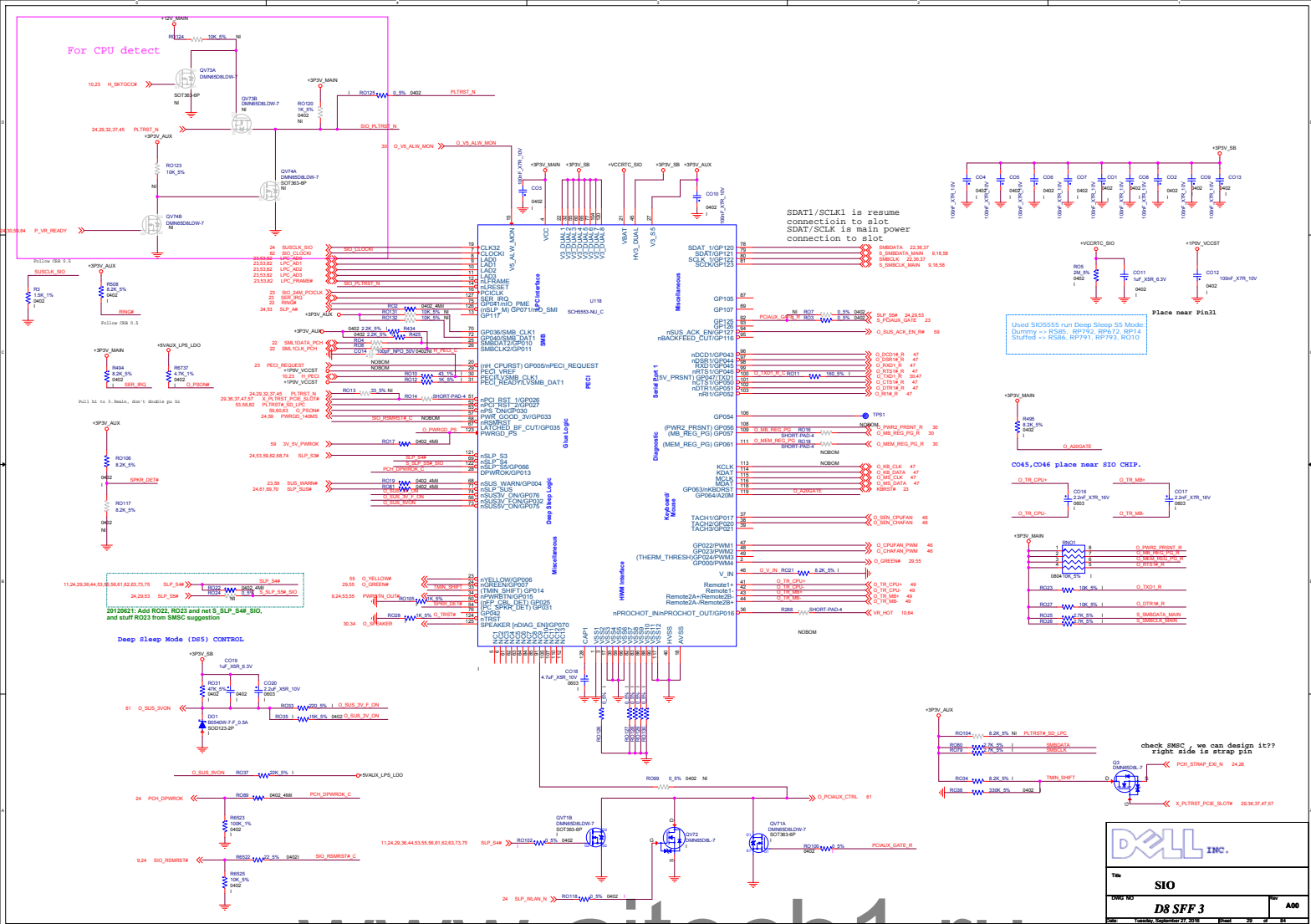
ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00



Chasis ID



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20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC




SIO5555 V5_ALW Monitor

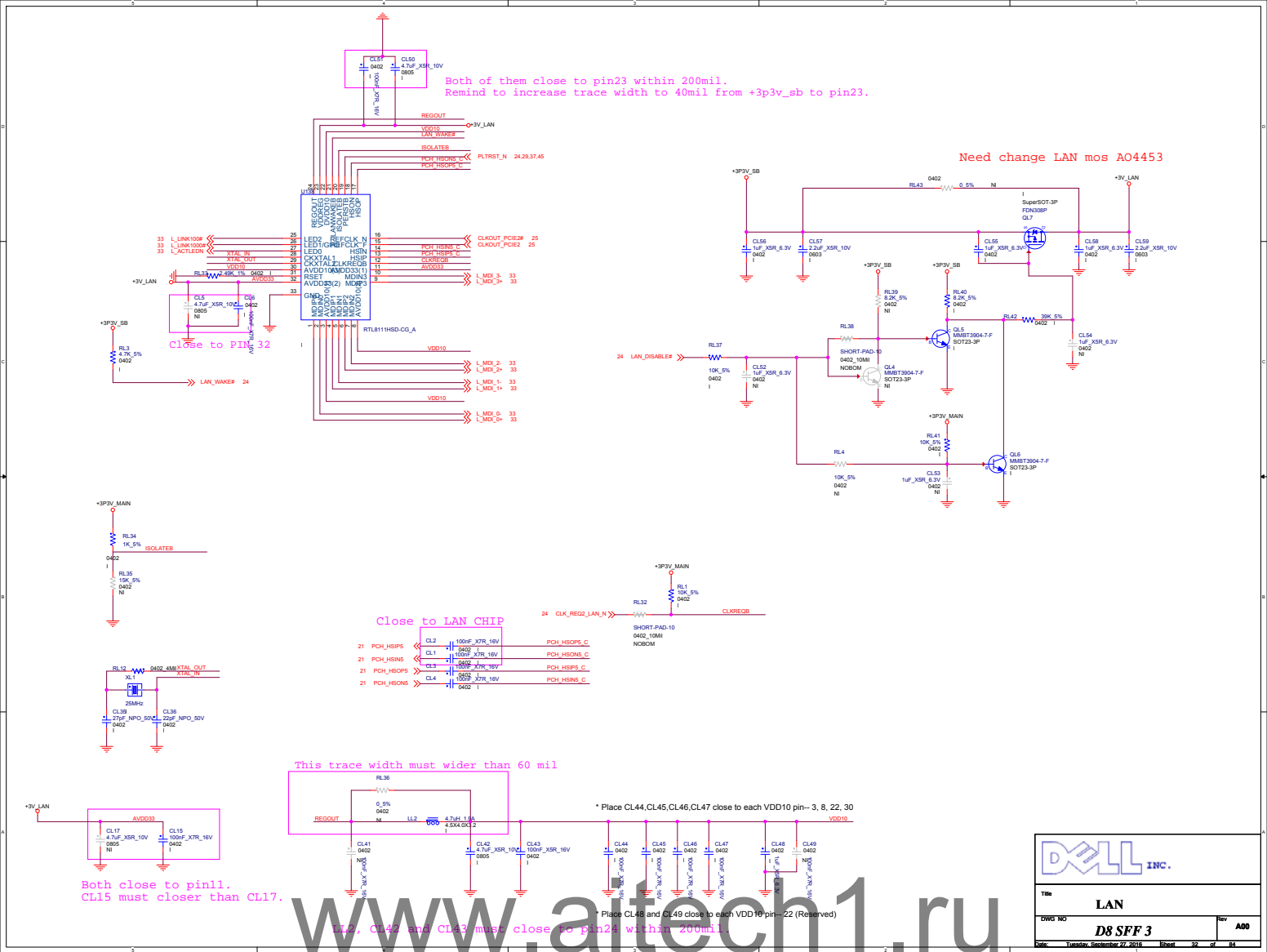


Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
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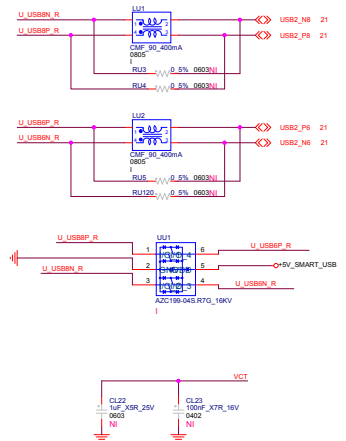
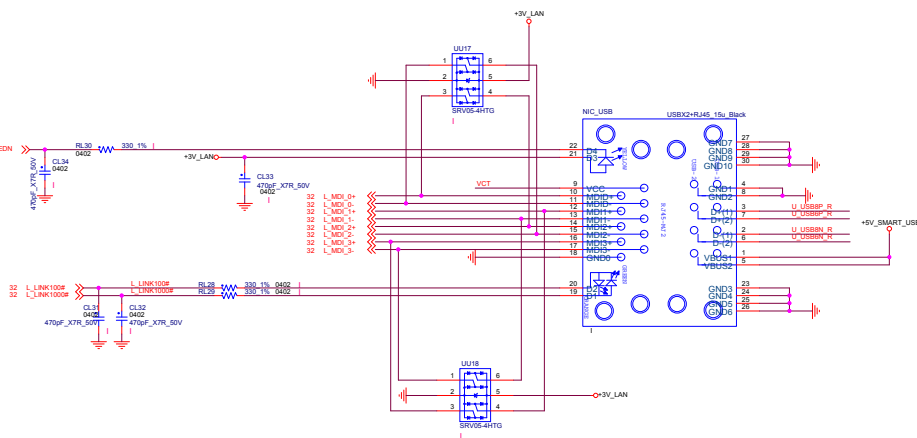
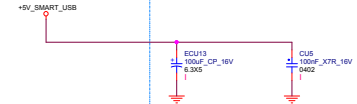
DELL INC.		
LAN		
DWG NO	D8 SFF 3	Rev A00
Date: Tuesday, September 27, 2016 Sheet 32 of 34		

+5V_SMART_USB

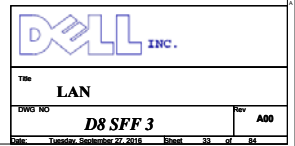


**20140521 Dell ARD1.01 Q&A
feedback : will support Smart USB
Conn on pair Rear USB2.0 port.**

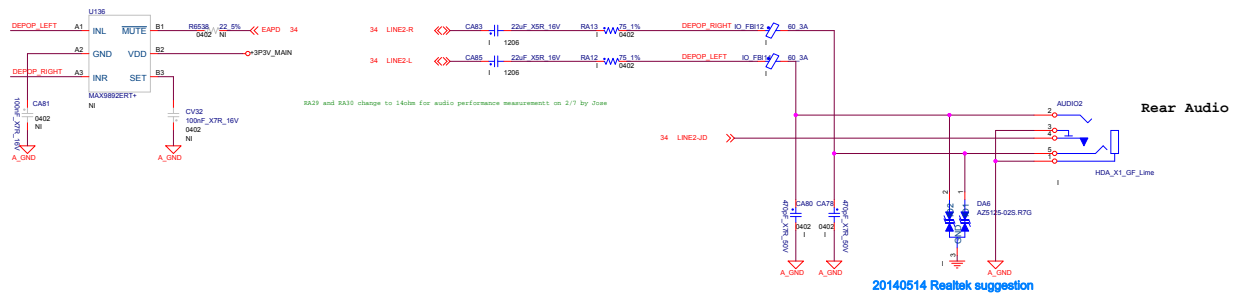
Remove FU1, ECU1, CU1, RU1, RU2



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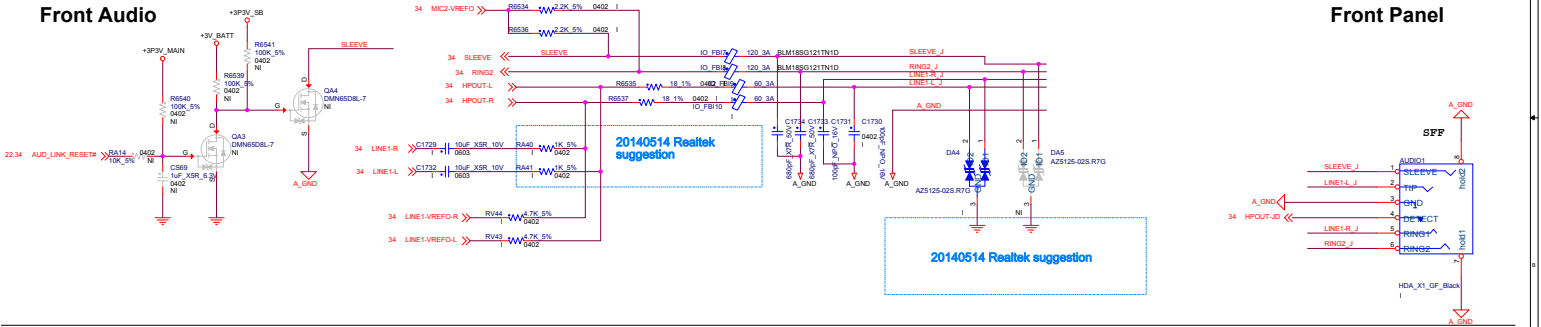


Rear Audio Jack

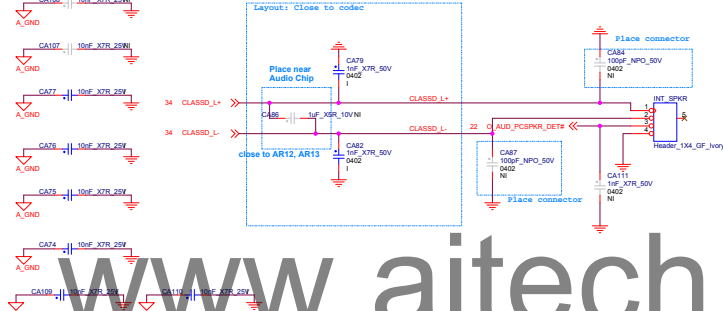
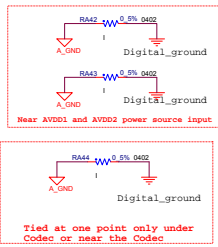


Front Audio

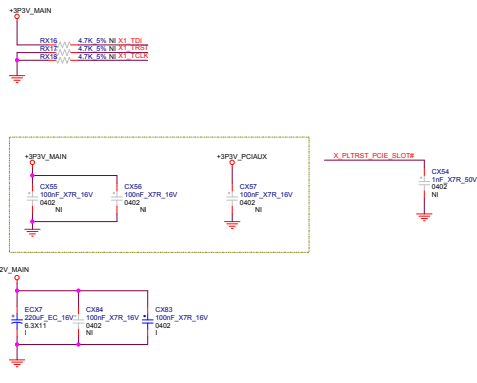
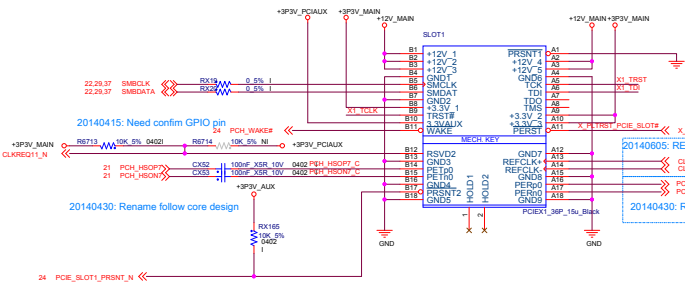
Front Panel



CHASSIS SPEAKER



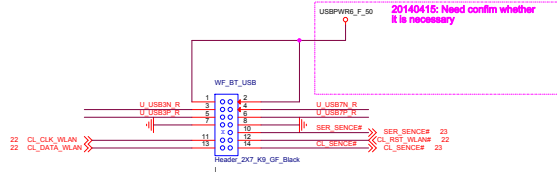
DELL INC.	
AUDIO	
DWG NO	Rev
D8 SFF 3	A00
Date: Tuesday, September 27, 2016	Sheet 35 of 81



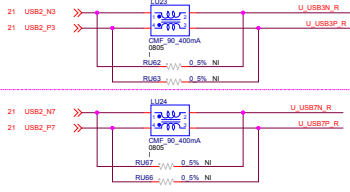
ARD 0.9 :Header populated on 7/9 series only
 Provides vPro and BT support from Intel wireless Add-in-Card
 USB and CLINK signals passed on cable from motherboard to Add-in-Card
 Compatible with standard USB 2.0 headers and cables

14 pin non shrouded header 0.1 pin spacing,
 Pin 14 allows sense of the CLINK/BT cable ,
 Add-in-Card does not use +5V_USB or USB2* (second port) signals

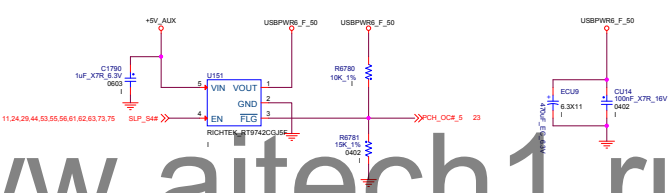
14 pin USB/CLINK Header				
+5V_USB	1	2	+5V_USB	
USB1N	3	4	USB2N	
USB1P	5	6	USB2P	
GND	7	8	GND	
Key (no pin)	9	10	SER_SENSE	
CLINK_CLK	11	12	CLINK_RST	
CLINK_DAT	13	14	CL_SENSE	



20140425 If for WLAN card only, it should be no need CMC

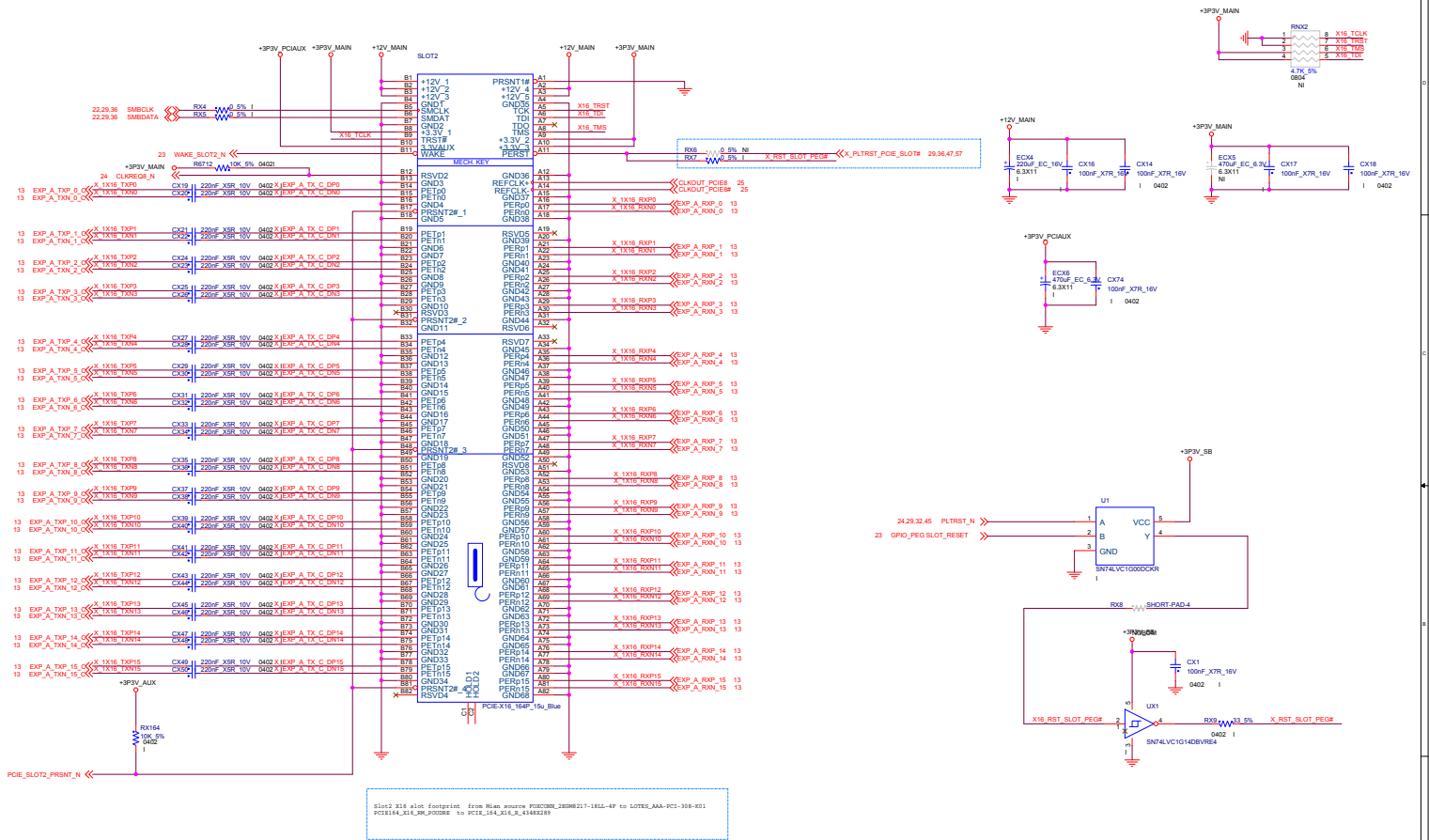


INT_USB1 USB2.0*2



PCIe 1x
D8 SFF 3
 Date: Tuesday, September 27, 2016 Sheet 36 of 81

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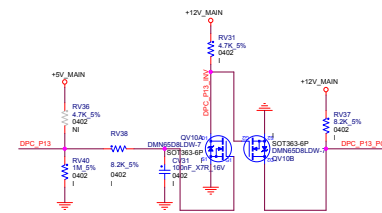
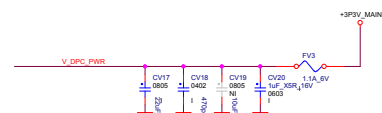
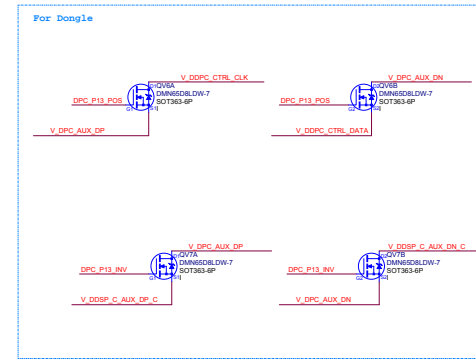
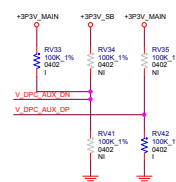
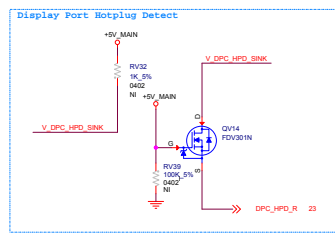
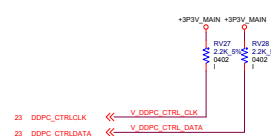
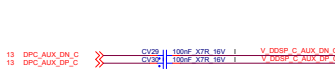
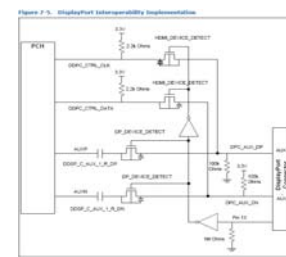
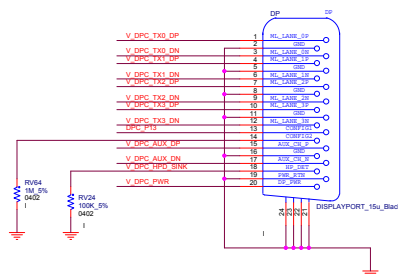
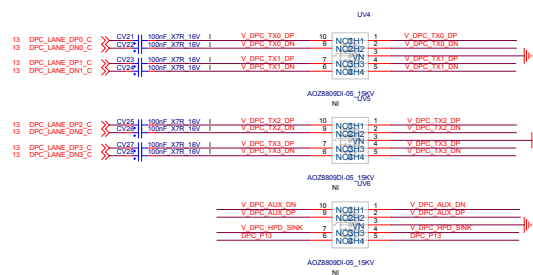
Title		
PCIe 16x		
DWG NO	Rev	A00
D8 SFF 3		
Date: Tuesday, September 27, 2016 Sheet 37 of 81		

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title	
CPU	
DWG NO	Rev
D8 SFF 3	A00
Date Tuesday, September 27, 2016 Sheet 38 of 81	

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Title		
Display Port -2		
DWG NO	D8 SFF 3	Rev
Date	Tuesday, September 27, 2016	Sheet 40 of 41

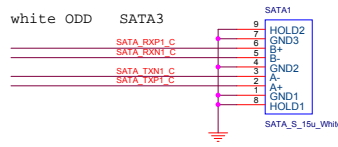
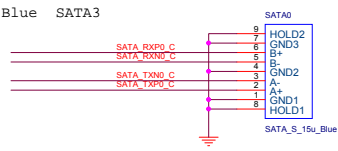
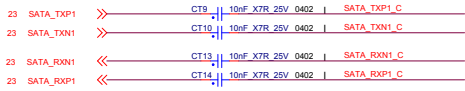
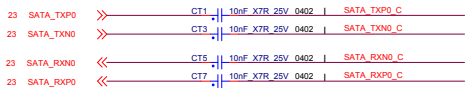
www.aitech1.ru

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
Date Tuesday, September 27, 2016 Sheet 41 of 84	


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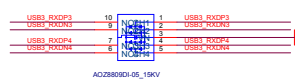
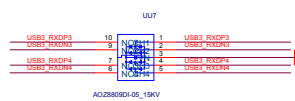
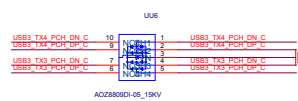
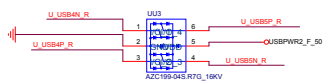
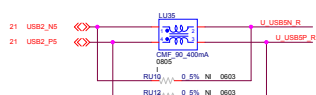
Title		
SATA Conn		
DWG NO	D8 SFF 3	Rev A00
Date: Tuesday, September 27, 2016	Sheet 42 of 84	

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
Date Thursday, September 27, 2018 Sheet 43 of 81	

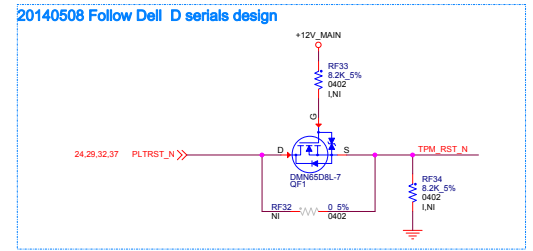
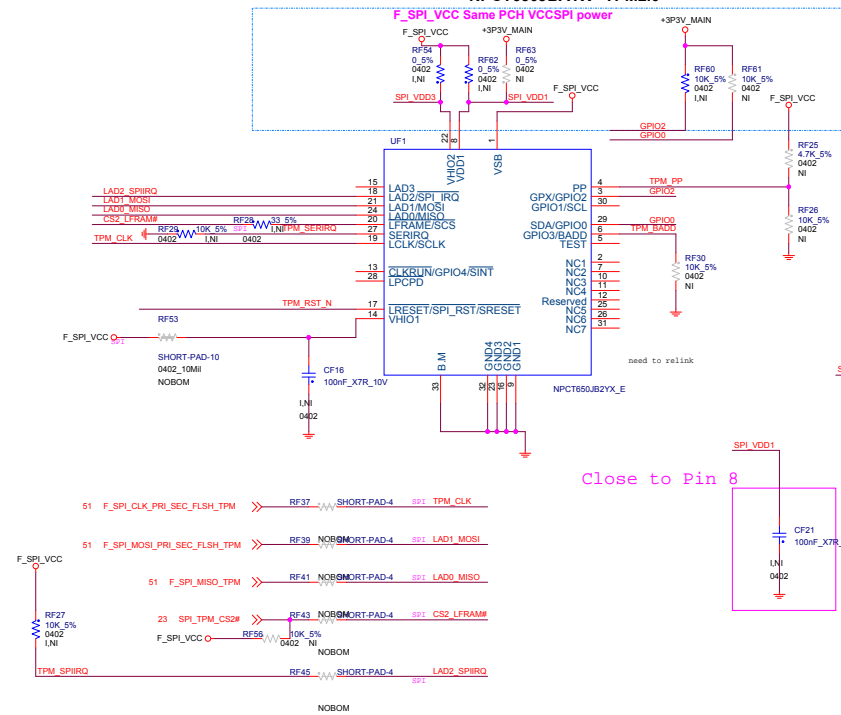
www.aitech1.ru

[illegible]

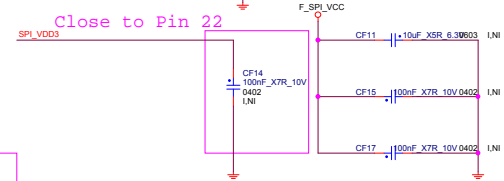
Trusted Computing Support

HW Low Power Mode	RF62	RF63	RF60
Support	Un-stuff	Stuff	Stuff
Not support	Stuff	Un-stuff	Un-stuff

Nuvoton NPCT650JB2YX TPM1.2 NPCT650JBAYX TPM2.0



Decoupling Capacitors

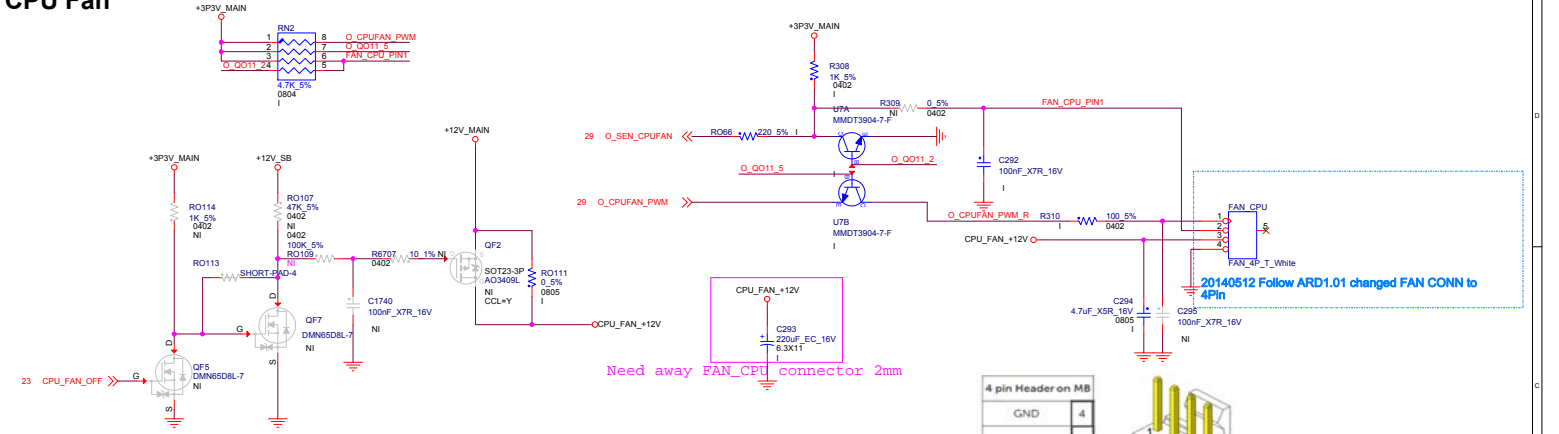


NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

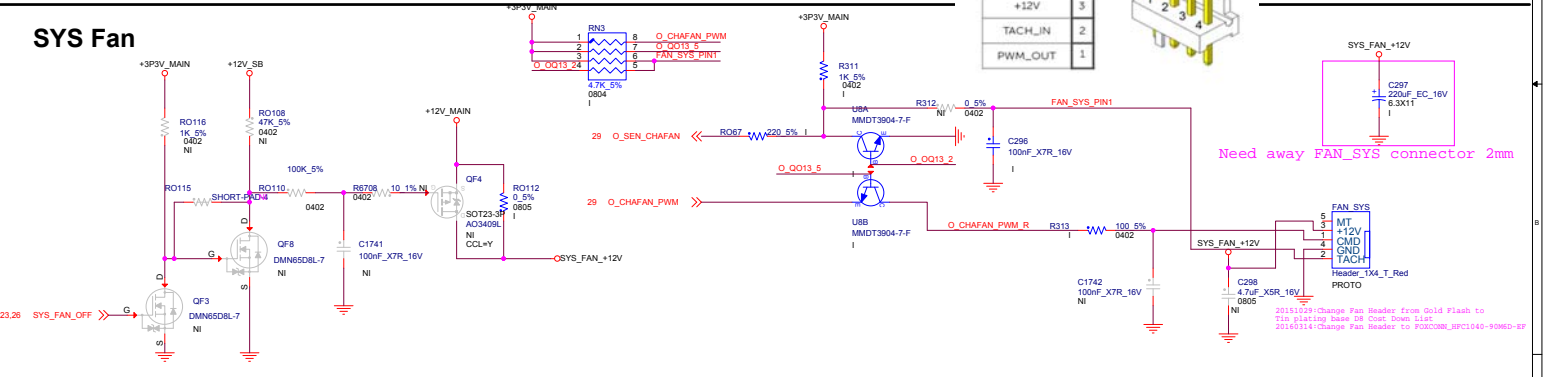
DELL INC.	
Title TPM	
DWG NO D8 SFF 3	Rev A00
Date: Tuesday, September 27, 2016	Sheet 45 of 84

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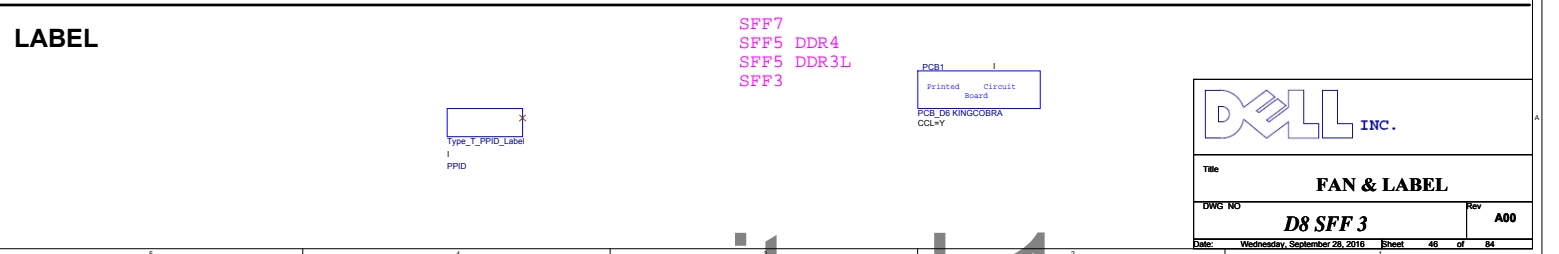
CPU Fan



SYS Fan



LABEL



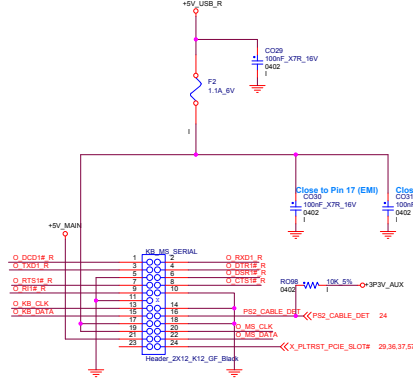
www.aitech1.ru

Serial Port 1

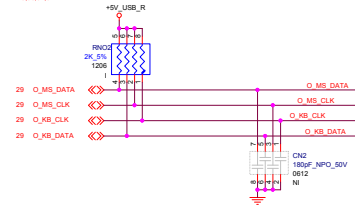
KB/MS

29 O_R18_R << O_R18_R
29 O_CTS14_R << O_CTS14_R
29 O_GSR14_R << O_GSR14_R
29 O_RTS14_R << O_RTS14_R
29 O_DTR14_R << O_DTR14_R
29 O_TXD1_R << O_TXD1_R
29 O_DCD14_R << O_DCD14_R

+5V_MAIN
C028
1000PF_XTR_16V
0402



20140512 Need check pin define




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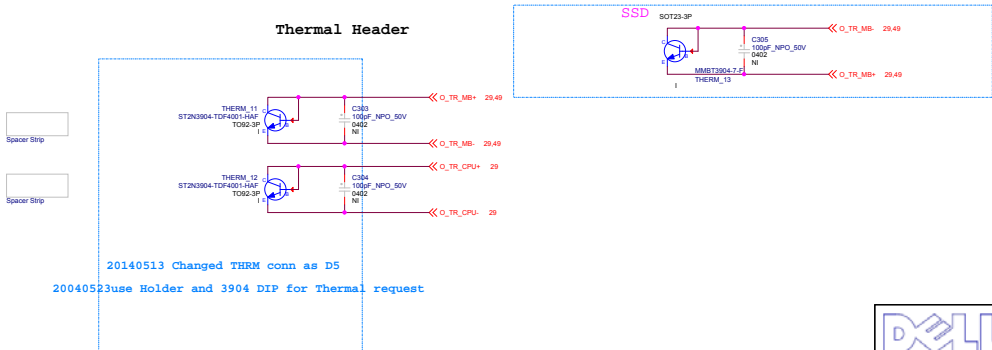
DELL INC.		
Title PS2 Conn		
DWG NO	D8 SFF 3	Rev A00
Date Tuesday, September 27, 2011	Sheet 47	of 81

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
Date Thursday, September 27, 2018 Sheet 08 of 08	

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DELL INC.


Title: **Thermal Sensor**

DWG NO: **D8 SFF 3** Rev: **A00**

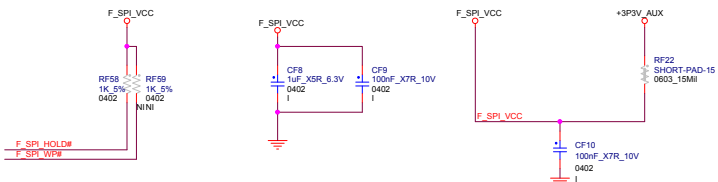
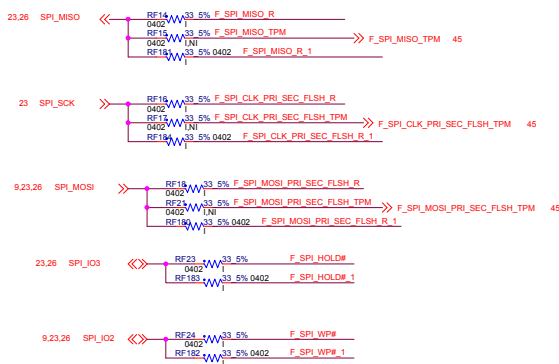
Date: **Tuesday, September 27, 2016** Sheet: **49** of **81**

Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
Date Tuesday, September 27, 2016 Sheet 50 of 81	

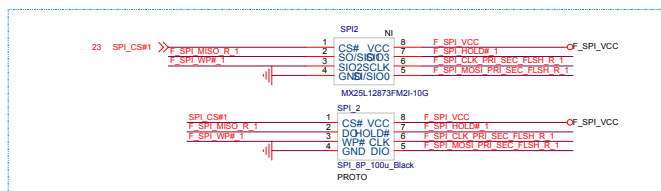
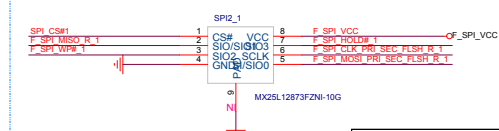
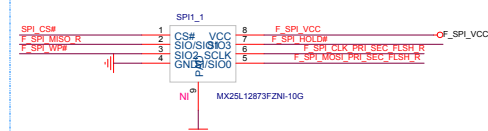
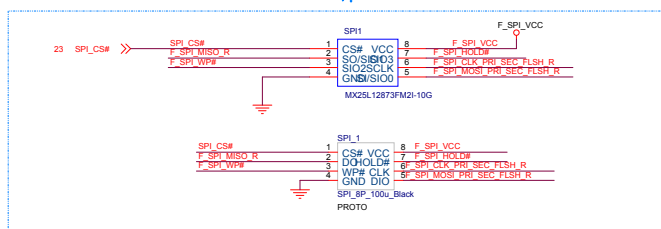
www.aitech1.ru



SPI_16MB

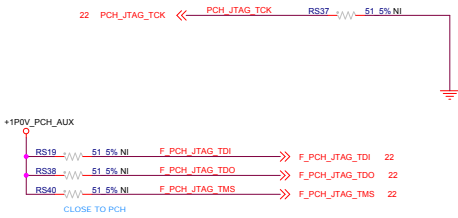
20140506 ARD0.92 : One SPI FLASH device site on PCB

Before RTS, please use DIP



Title		
SPI		
DWG NO		Rev
D8 SFF 3		A00
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20140505 Remove Duplicated XDP

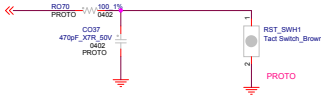


Title		
XDP		
DWG NO	D8 SFF 3	Rev A00
Date: Tuesday, September 27, 2016	Sheet 52	of 84

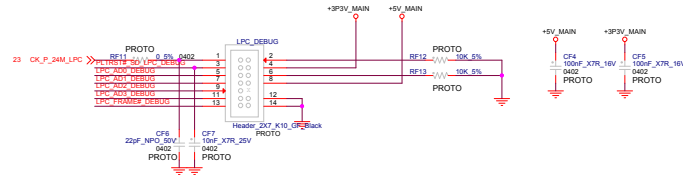
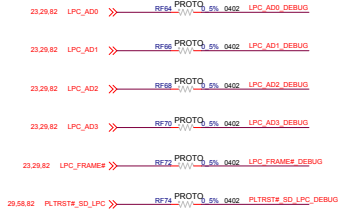
Power Bottom



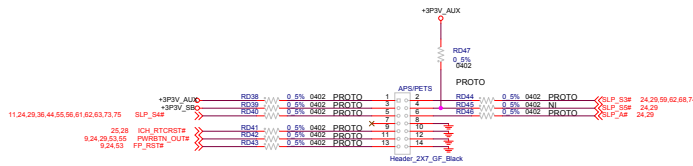
Reset Bottom



LPC DEBUG



APS Debug



Debugging		
APS Connector	Pin	Alternate
Pin 1	VccSW3_3	3.3 V Suspended Power Web
Pin 2	SLP_S38	When asserted (0) system is in S3
Pin 3	VccSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSW3_3	When off (0) system is in S5
Pin 5	SLP_S48	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Muff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCRES#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRES#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

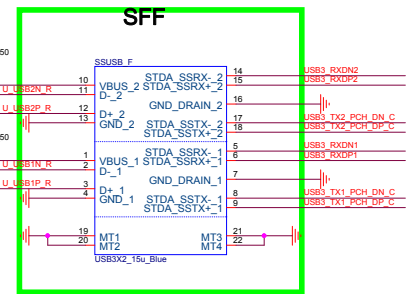
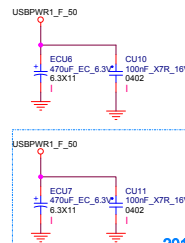
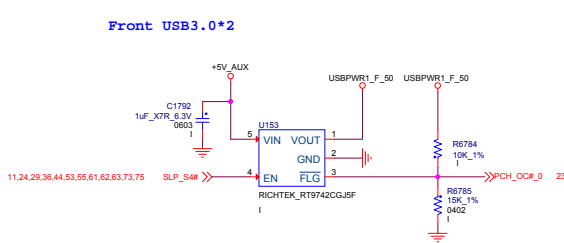


Pilot Run Conn		
DWG NO	Rev	Rev
D8 SFF 3	A00	
Date: Tuesday, September 27, 2016 Sheet 53 of 81		

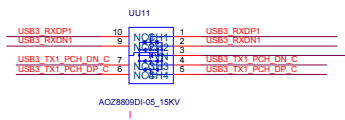
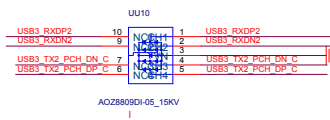
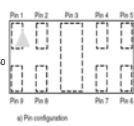
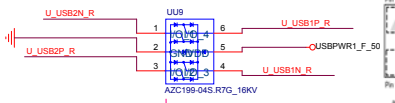
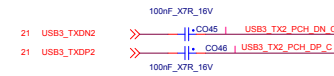
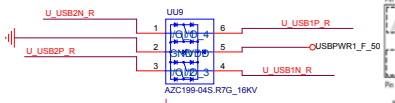
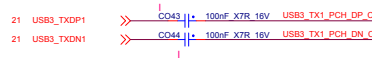
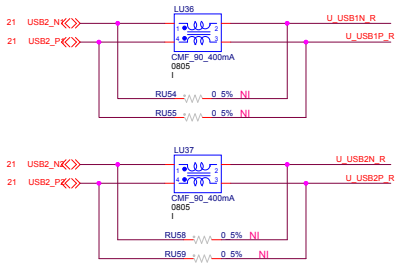
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Front USB/LED Header

Front USB3.0*2



20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

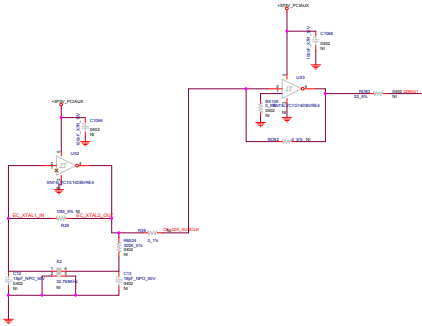
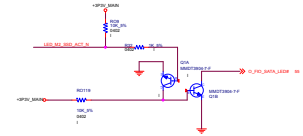
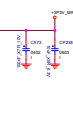
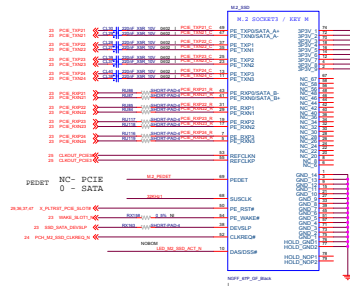


Title		
FRONT_USB3.0		
DWG NO	D8 SFF 3	Rev A00
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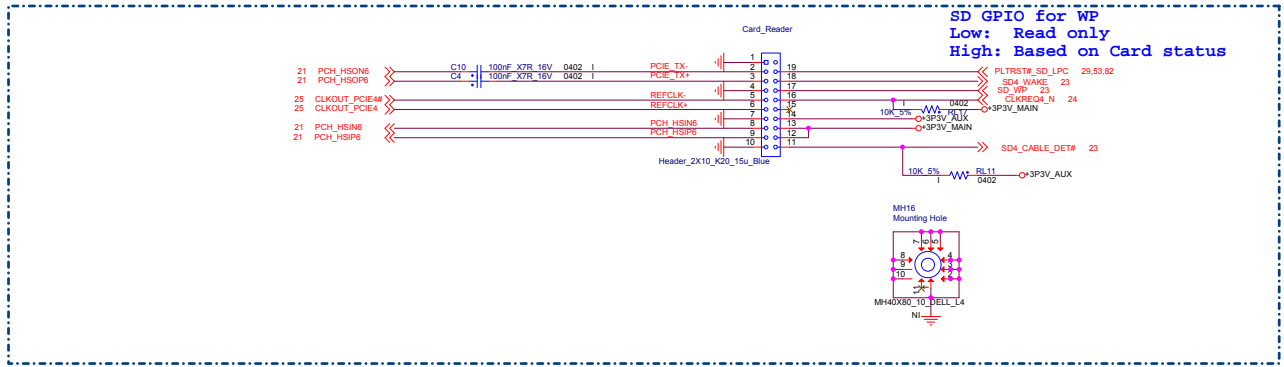


Spacer



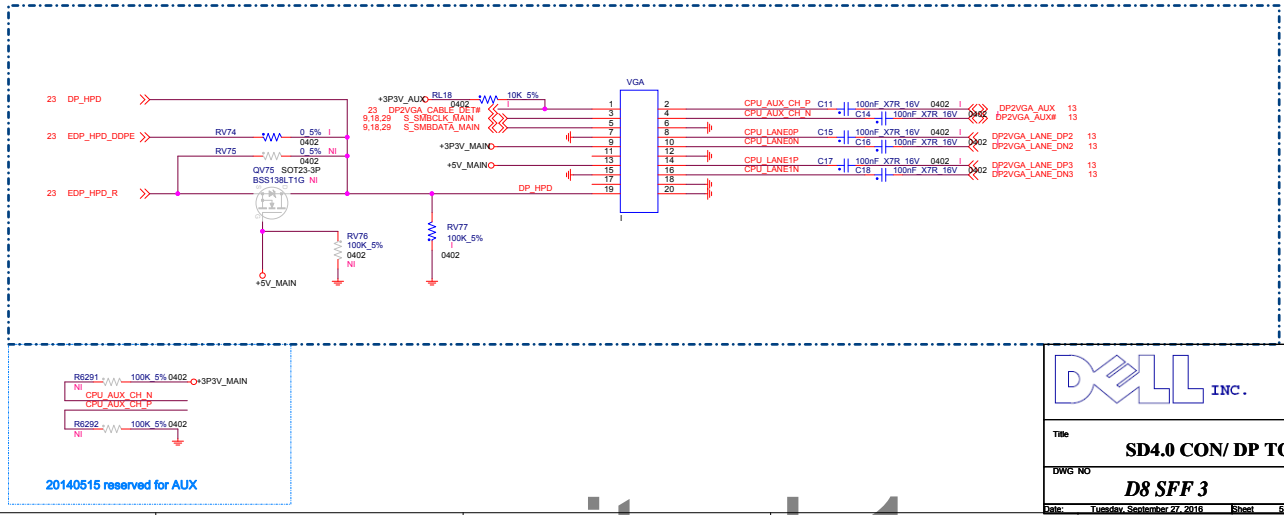
www.aitech1.ru

SD4.0 CONN



eDP to VGA CONN

M/B part already OK

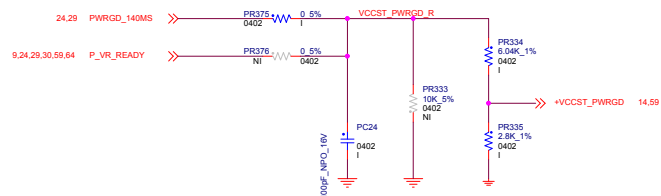
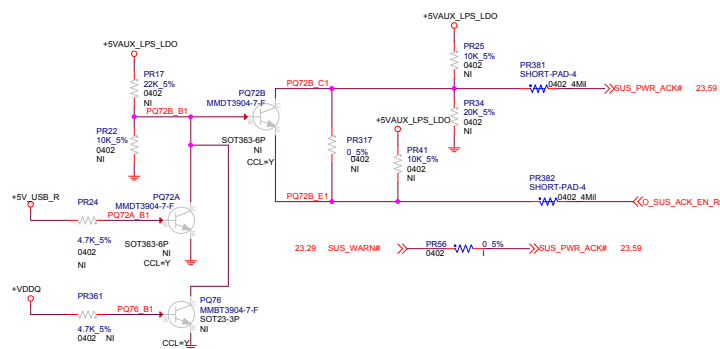


DELL INC.

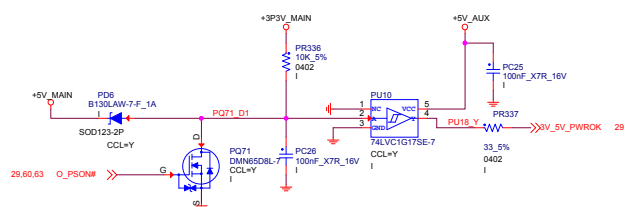
Title		
SD4.0 CON/ DP TO VGA CON		
DWG NO	Rev	
D8 SFF 3	A00	
Date	Tuesday, September 27, 2016	Sheet 58 of 84

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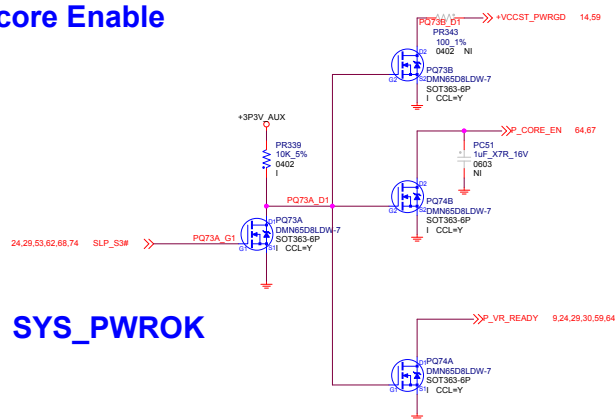
VCCST_PWRGD/PCH_PWROK



Power Sequence



Vcore Enable



SYS_PWROK



Title **Power Sequence**

DWG NO
D8

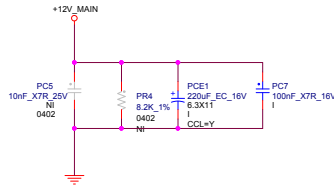
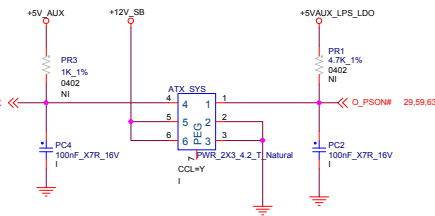
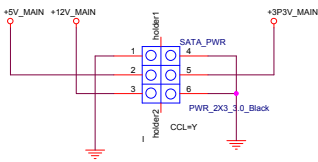
Date: Tuesday, September 27, 2016 She

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ATX POWER CONNECTOR

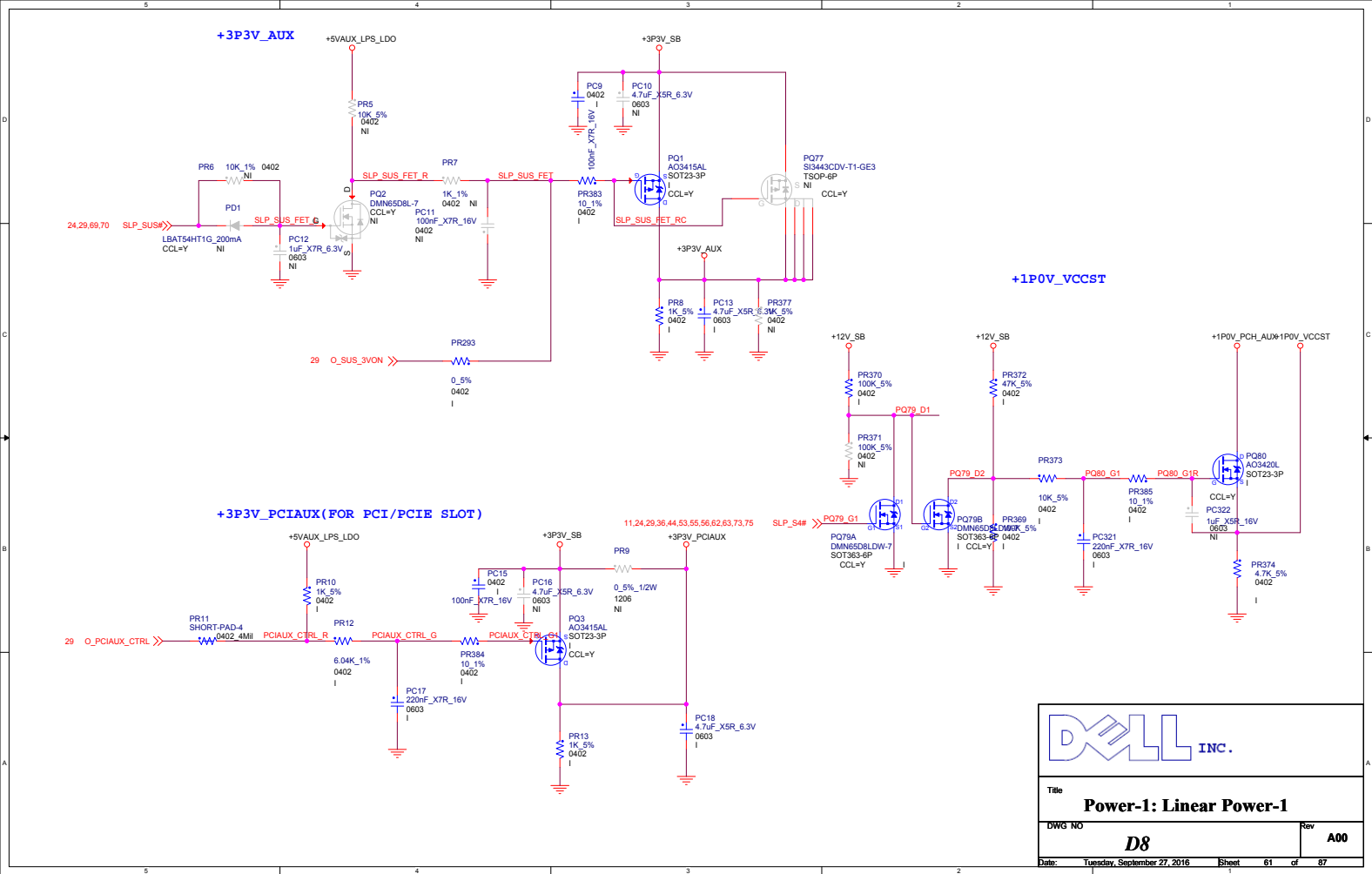


For ODD and HDD For SFF



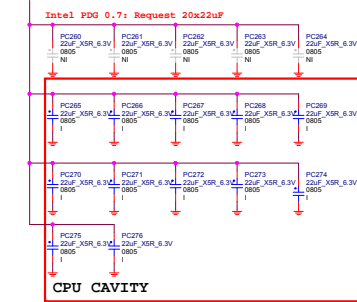
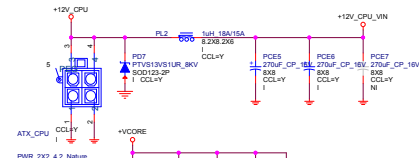
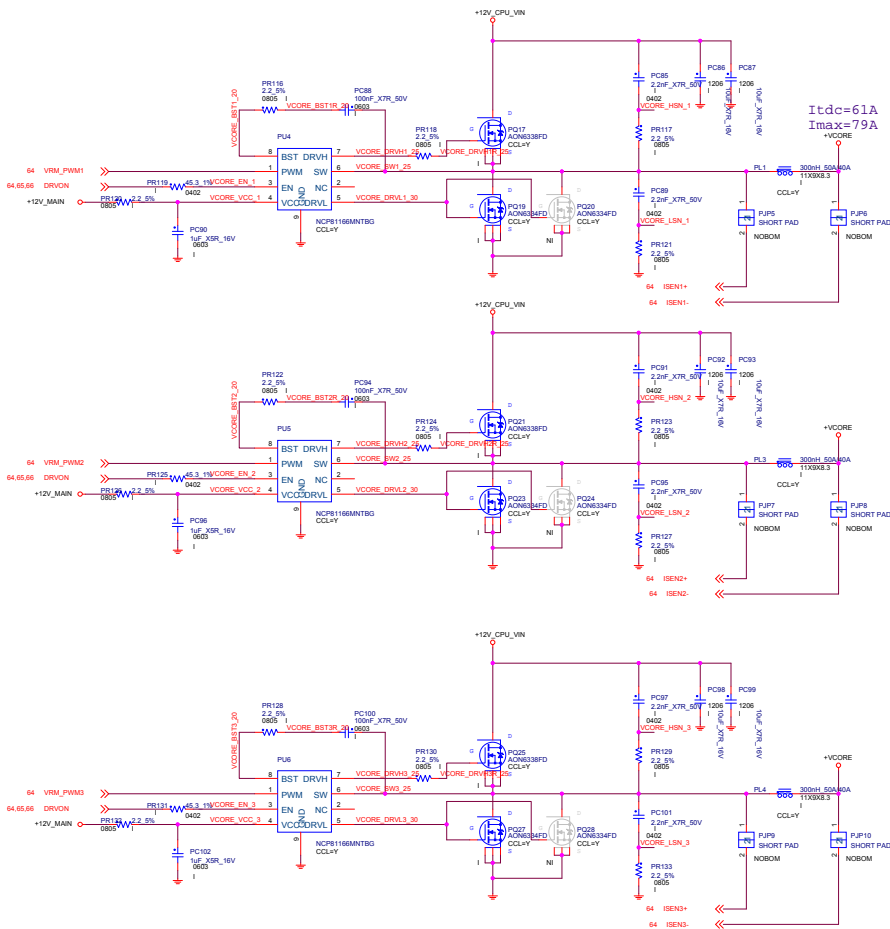
Title		
Power CONN		
DWG NO	D8	Rev A00
Date	Tuesday, September 27, 2016	Sheet 60 of 87

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VCORE PHASE1-3



CPU CAVITY

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

Vcore_VCC

Vcore_DRV

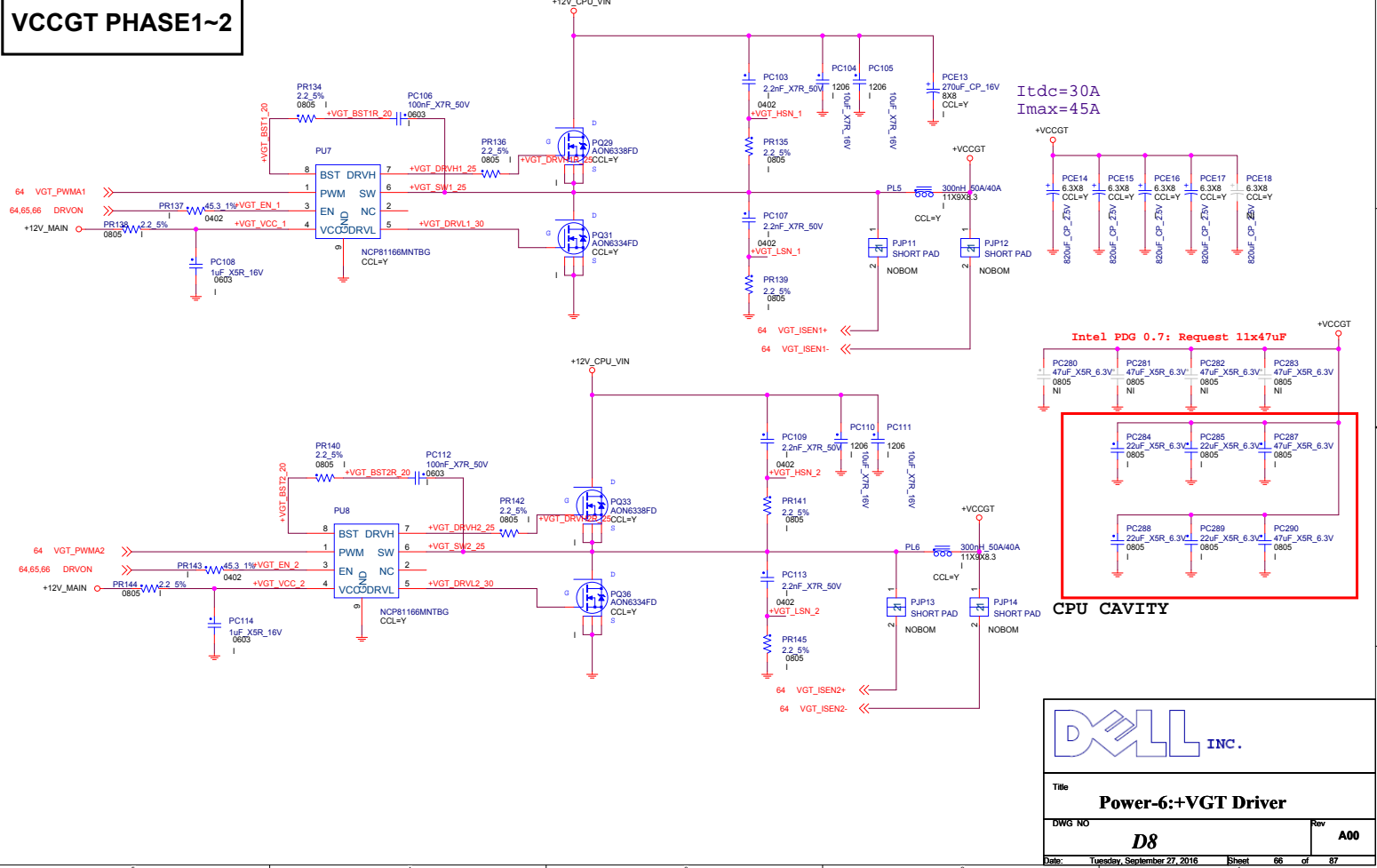
Vcore_VCC

Vcore_DRV

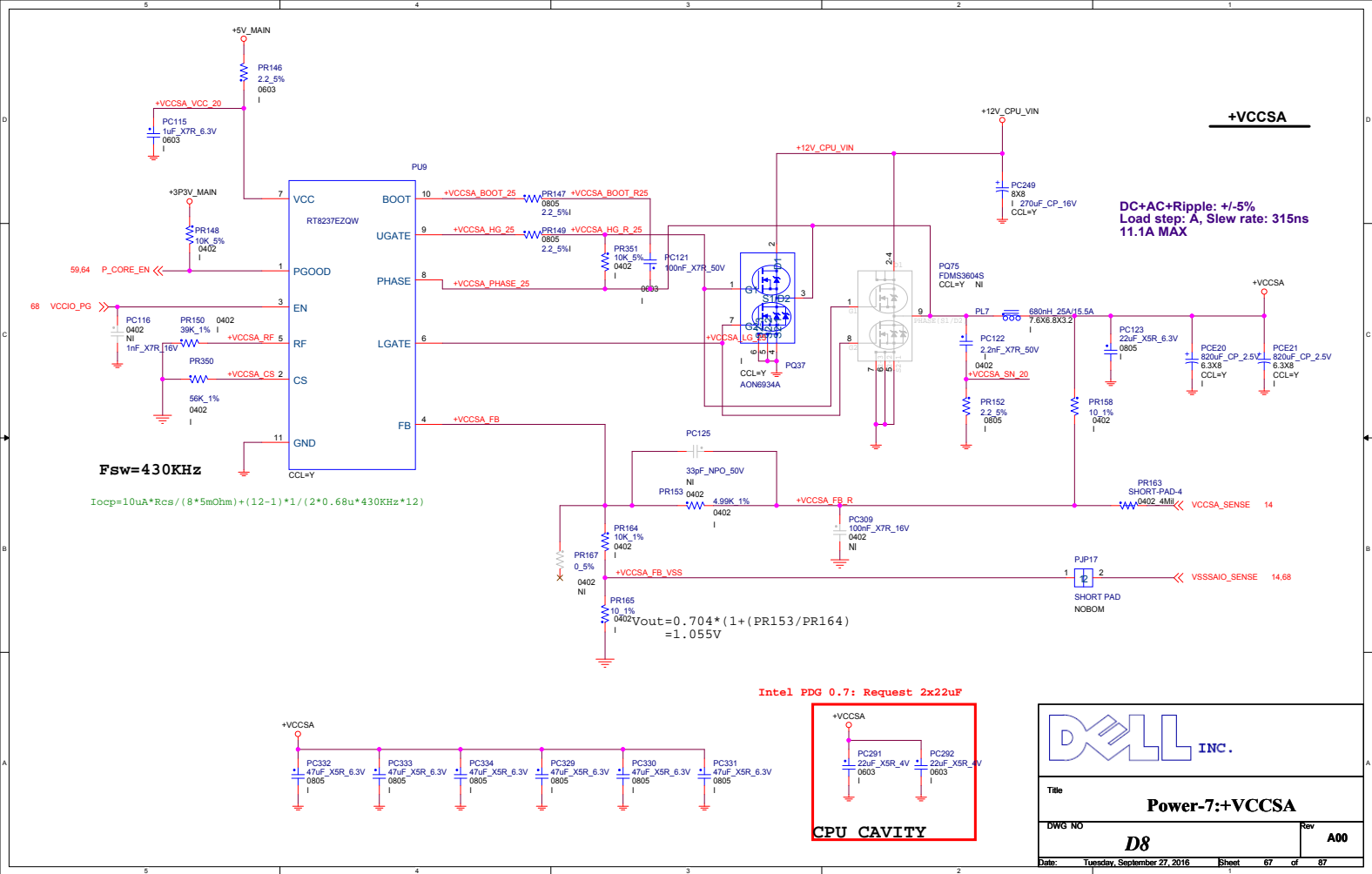
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DELL INC.		
Title Power-S:+Vcore Driver		
Doc No	D8	Rev A00
Date	Wednesday, September 27, 2016	Print 65 87

VCCGT PHASE1~2

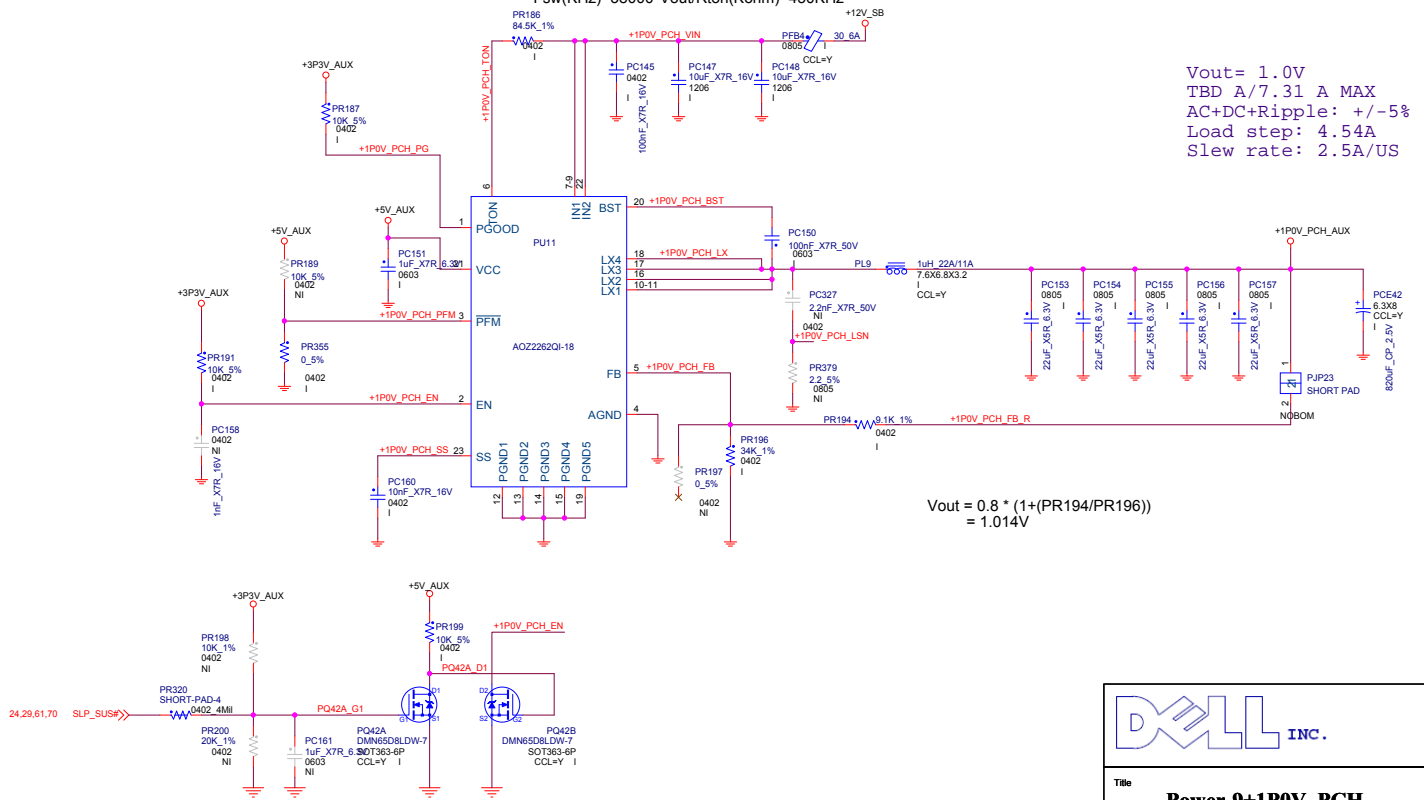


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+1P0V_PCH_AUX

$$F_{sw}(KHz) = 38000 \cdot V_{out} / R_{ton}(Kohm) = 450 KHz$$


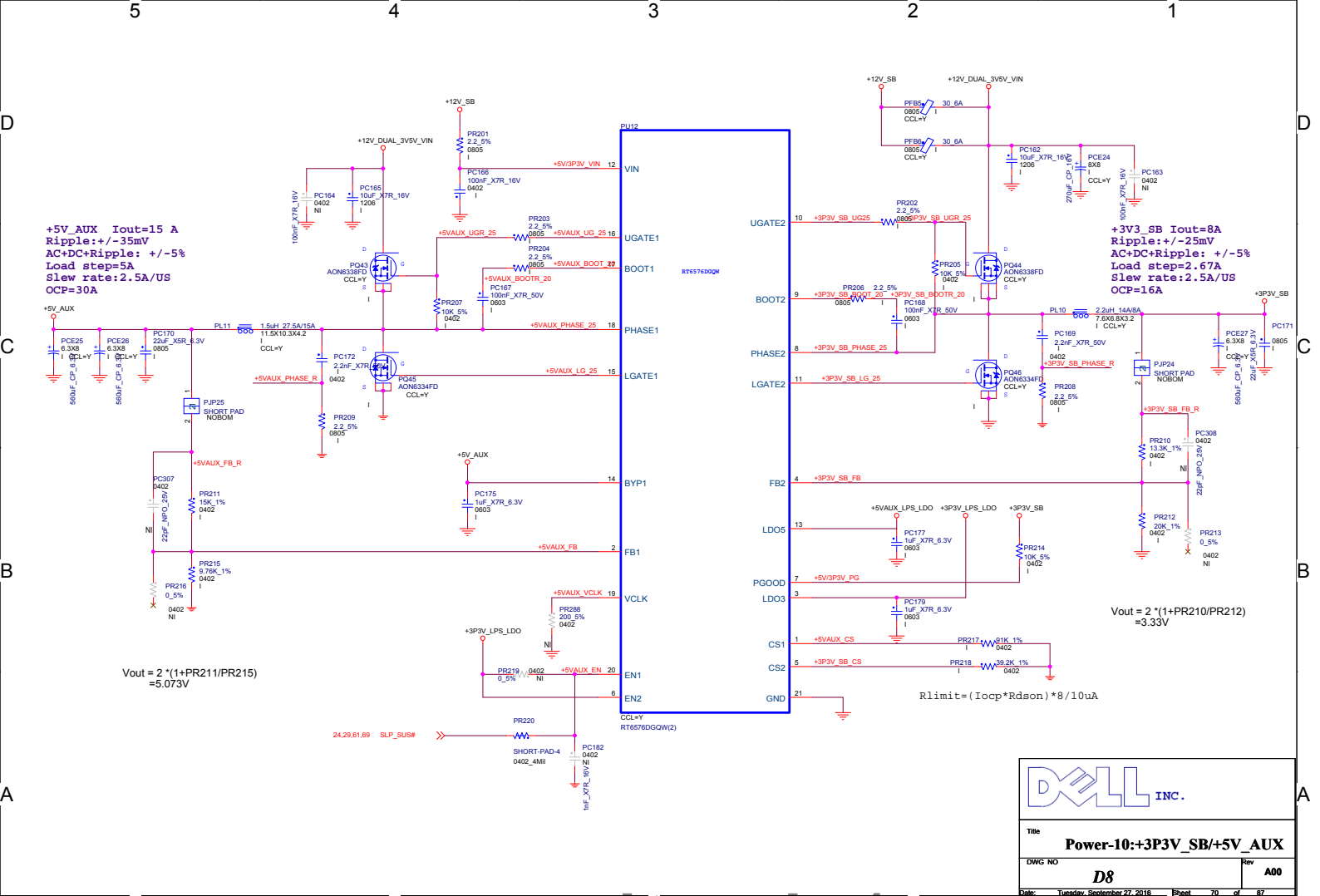
Vout= 1.0V
TBD A/7.31 A MAX
AC+DC+Ripple: +/-5%
Load step: 4.54A
Slew rate: 2.5A/US


$$V_{out} = 0.8 * (1 + (PR194/PR196))$$
$$= 1.014V$$



Title	Power-9+1P0V_PCH
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DWG NO	Rev
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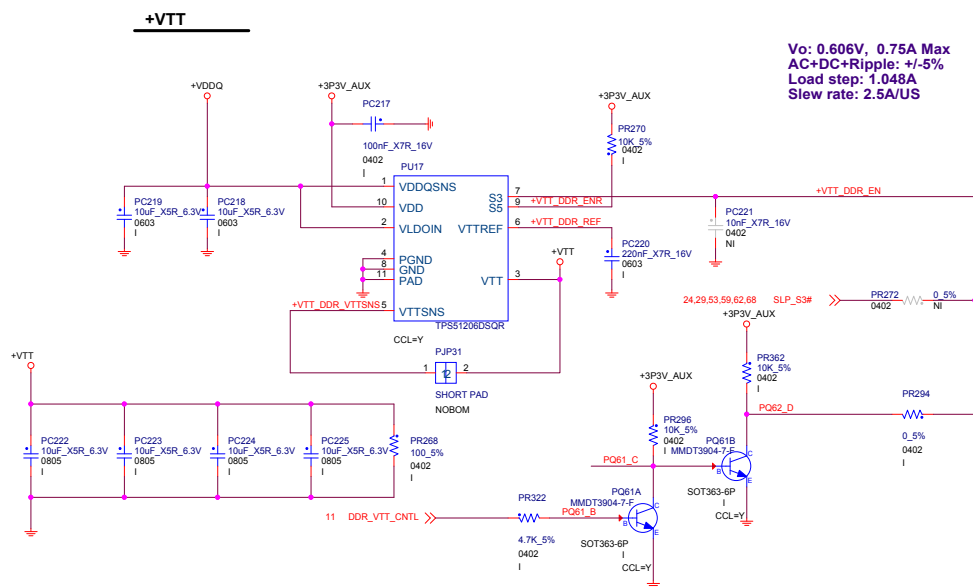


 INC.	
Title Power-11:-12V	
DWG NO D8	Rev A00
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Title TBD	
DWG NO D8	Rev A00
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DELL INC.	
Title	
Power-15:DDR4 +VTT_DDR	
DWG NO	Rev
D8	A00
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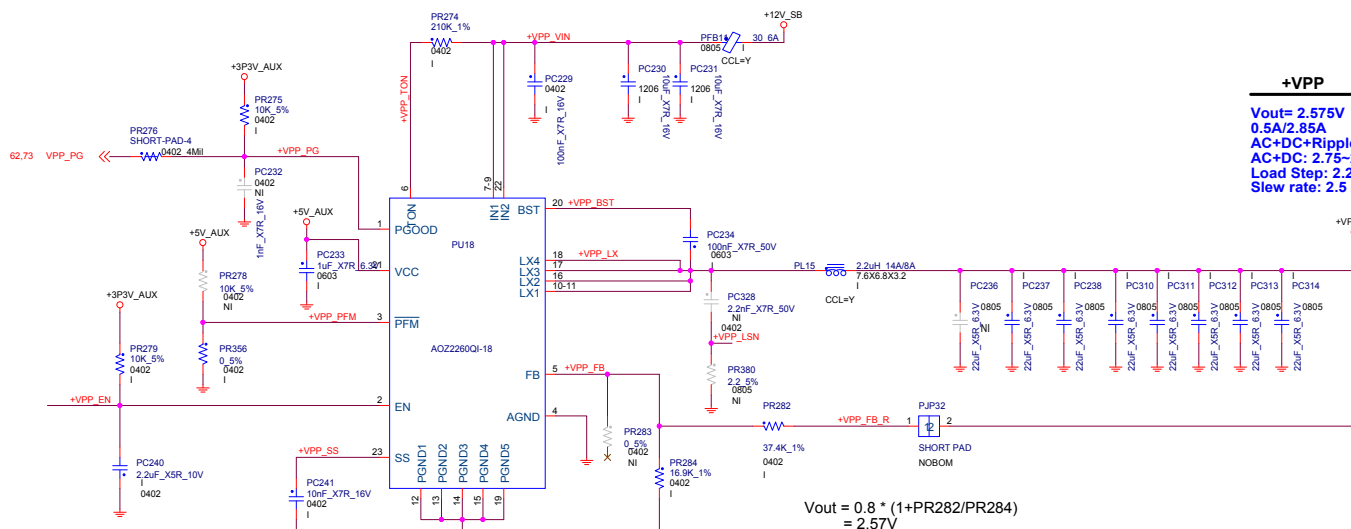
www.aitech1.ru

+VPP

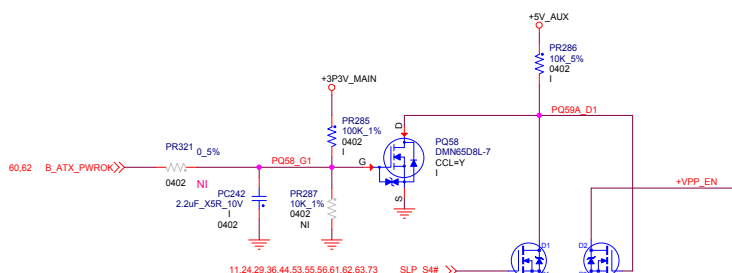
Fsw(KHz)=38000*Vout/Rton(Kohm)=450KHz

+VPP

Vout= 2.575V
0.5A/2.85A
AC+DC+Ripple: +/-50mV
AC+DC: 2.75~2.41V
Load Step: 2.2A
Slew rate: 2.5 A/US



$$V_{out} = 0.8 * (1 + PR282/PR284) = 2.57V$$



DELL INC.		
Title Power-16:DDR4 +VPP		
DWG NO D8	Rev A00	
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Title	
DDR3 Conn: CHA_1 (DIMM3)	
Doc No	Rev
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Intel PCH XDP Debug Connector

Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
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Title DDR3 Conn: CHB_1 (DIMM4)	
DWG NO D8 SFF 3	Rev A00
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Intel PCH XDP Debug Connector


Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
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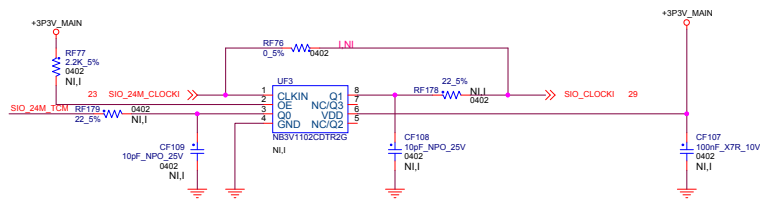
www.aitech1.ru

Intel PCH XDP Debug Connector

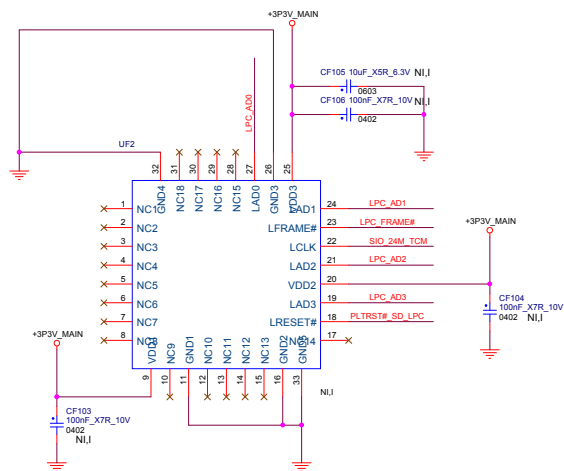
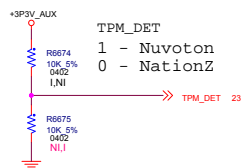
Project	
Spitfire	V
Scorpion	V
Toledo	V

	
Title CPU	
DWG NO D8 SFF 3	Rev A00
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23,29,53 LPC_AD0 >> LPC_AD0
 23,29,53 LPC_AD1 >> LPC_AD1
 23,29,53 LPC_AD2 >> LPC_AD2
 23,29,53 LPC_AD3 >> LPC_AD3
 23,29,53 LPC_FRAME# >> LPC_FRAME#
 29,53,58 PLTRST#_SD_LPC >> PLTRST#_SD_LPC




Title		
TPM (NationZ)		
DWG NO	Rev	
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Title VGA on board	
DMC NO D8 SFF 3	Rev A00
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Title	
VGA DP header	
DWG NO	Rev
D8 SFF 3	A00
Date Tuesday, September 27, 2016	
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